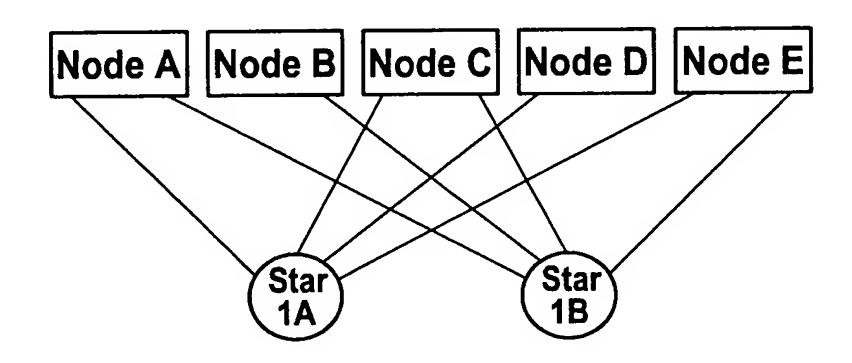
Fig. 1

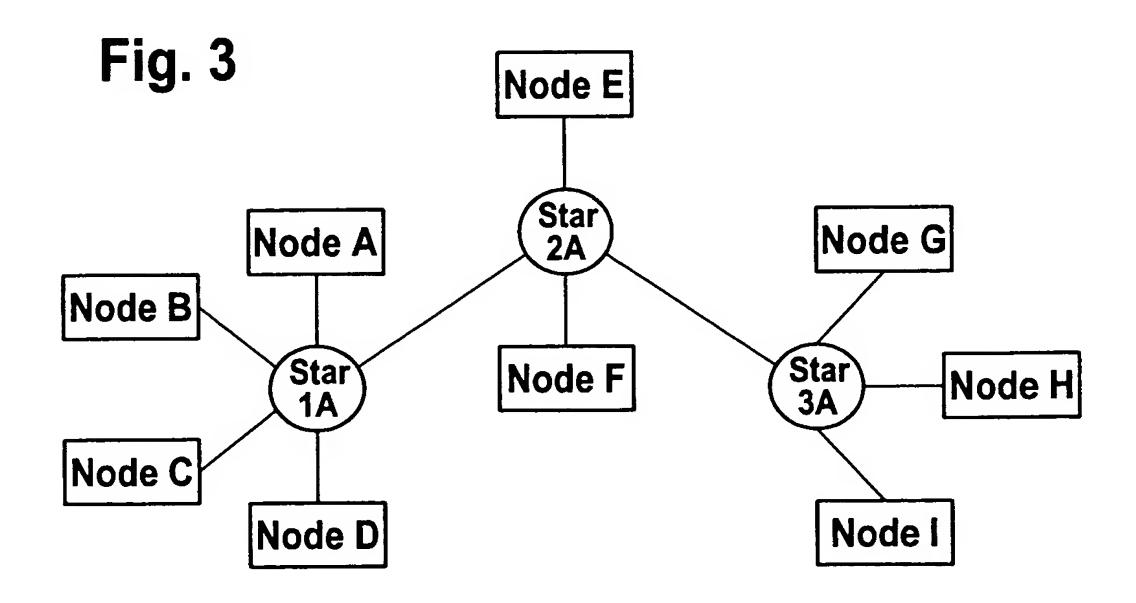
100

Node A Node B Node C Node D Node E

Channel A

Fig. 2





Channel B

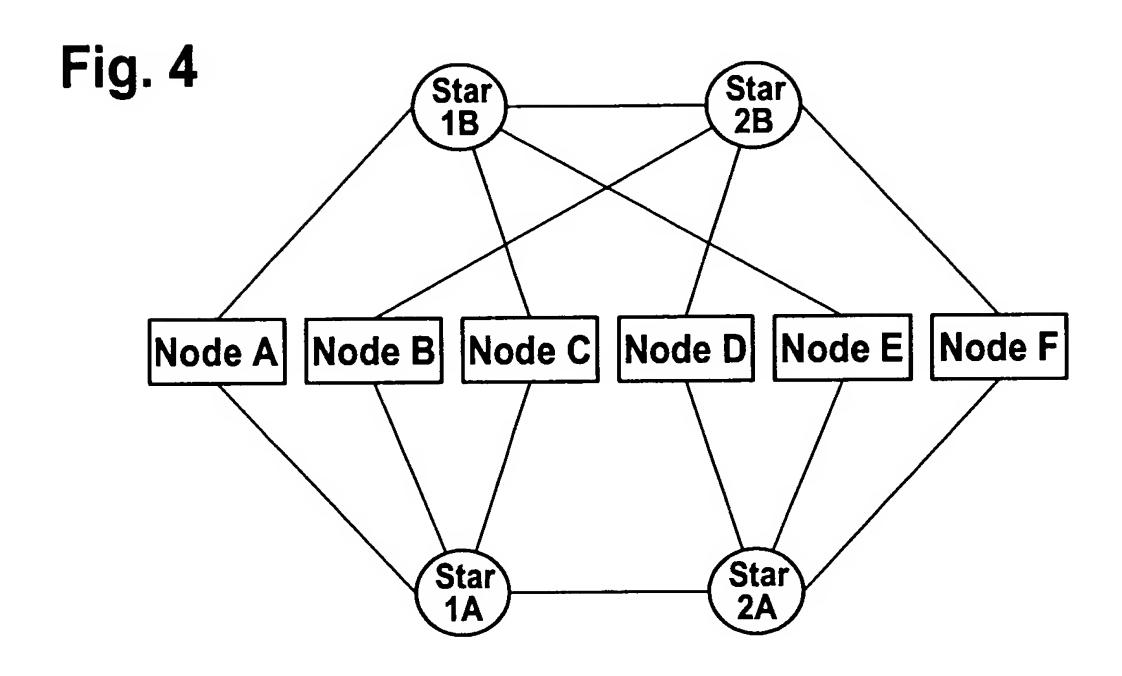


Fig. 5

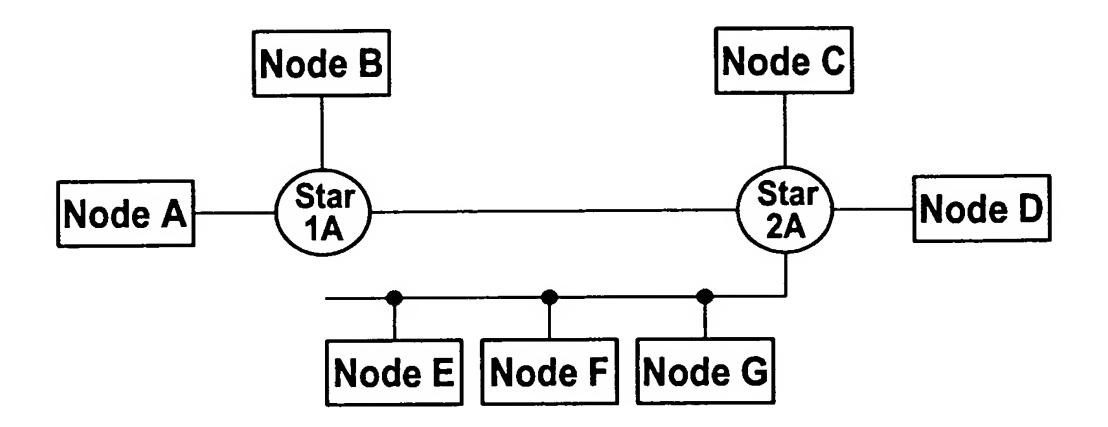


Fig. 6

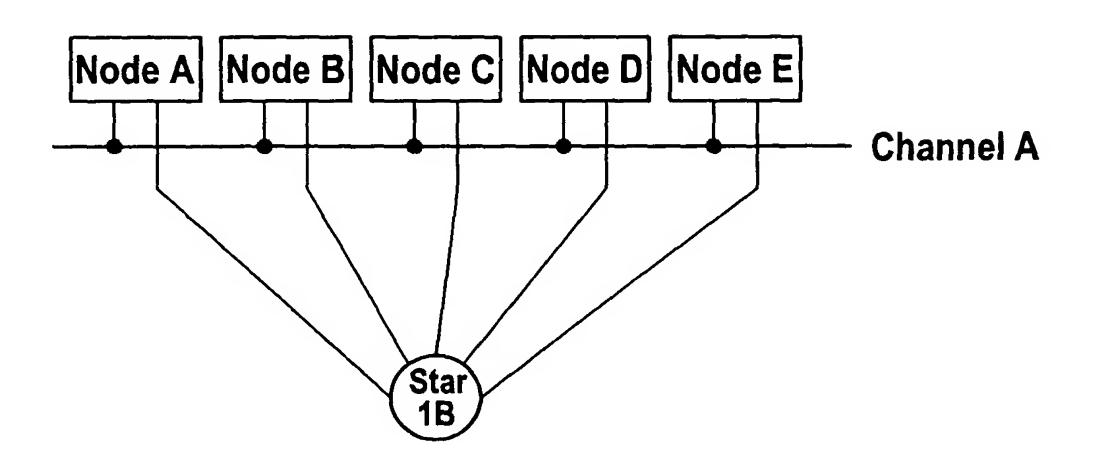


Fig. 7

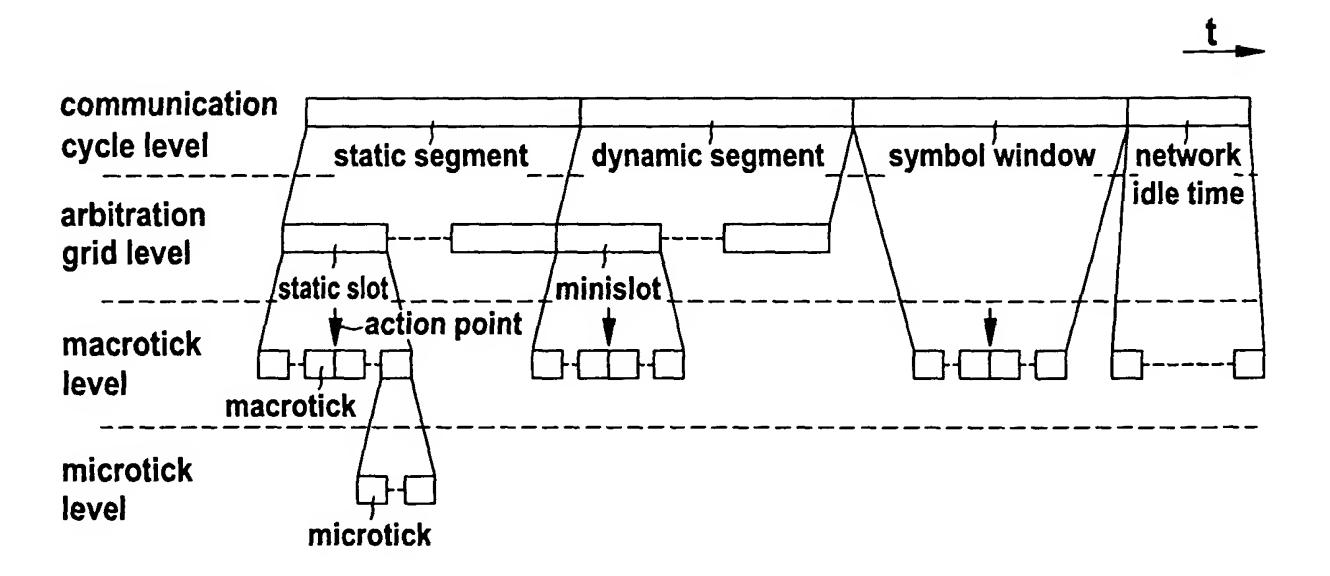


Fig. 8

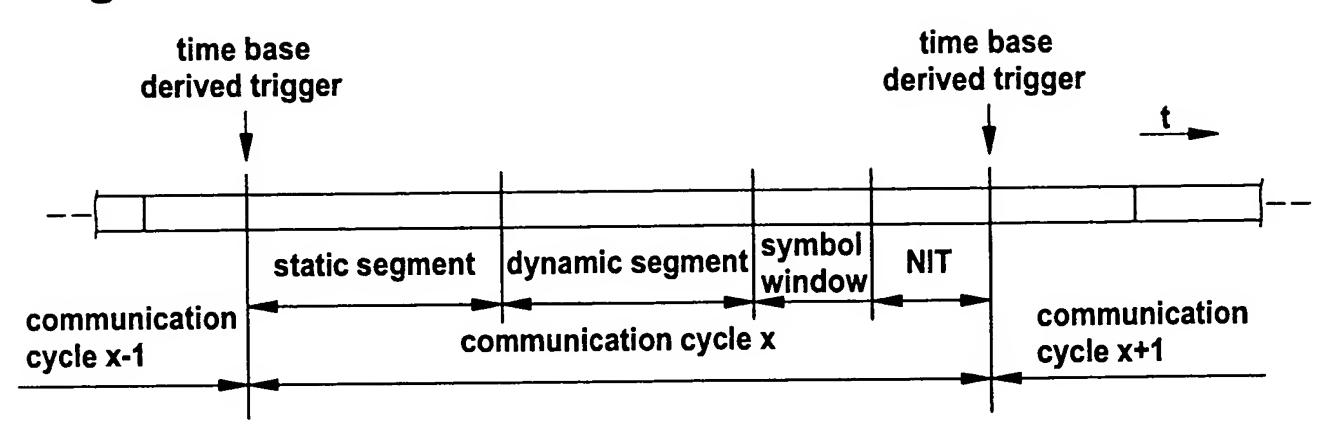


Fig. 9

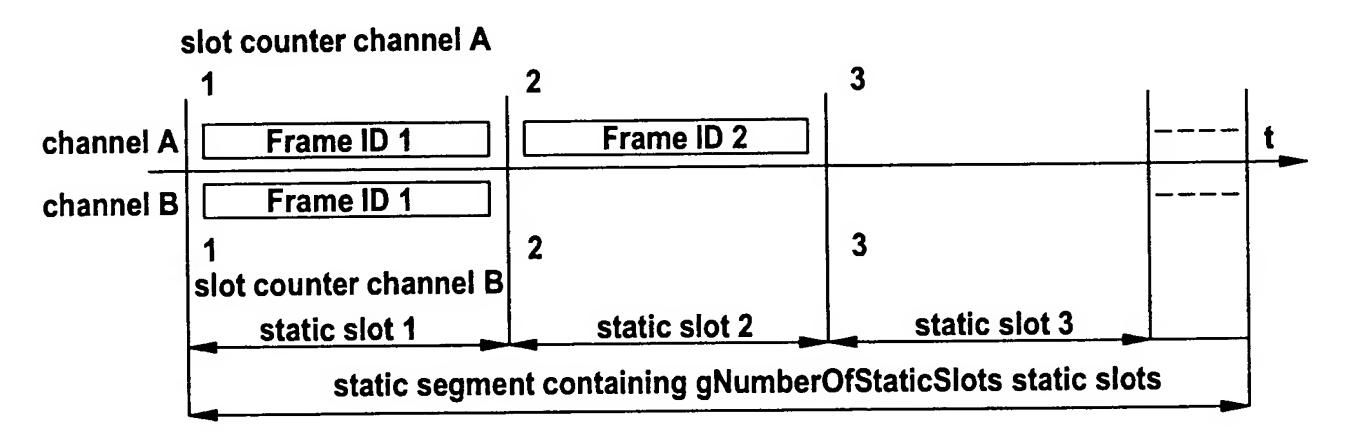
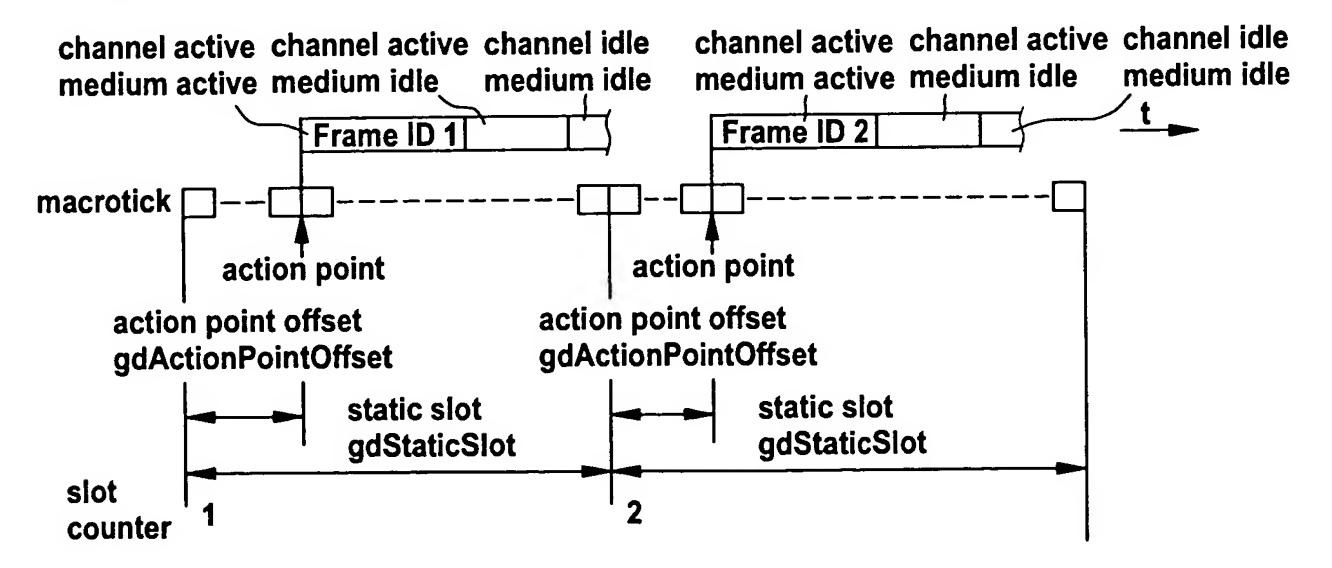


Fig. 10



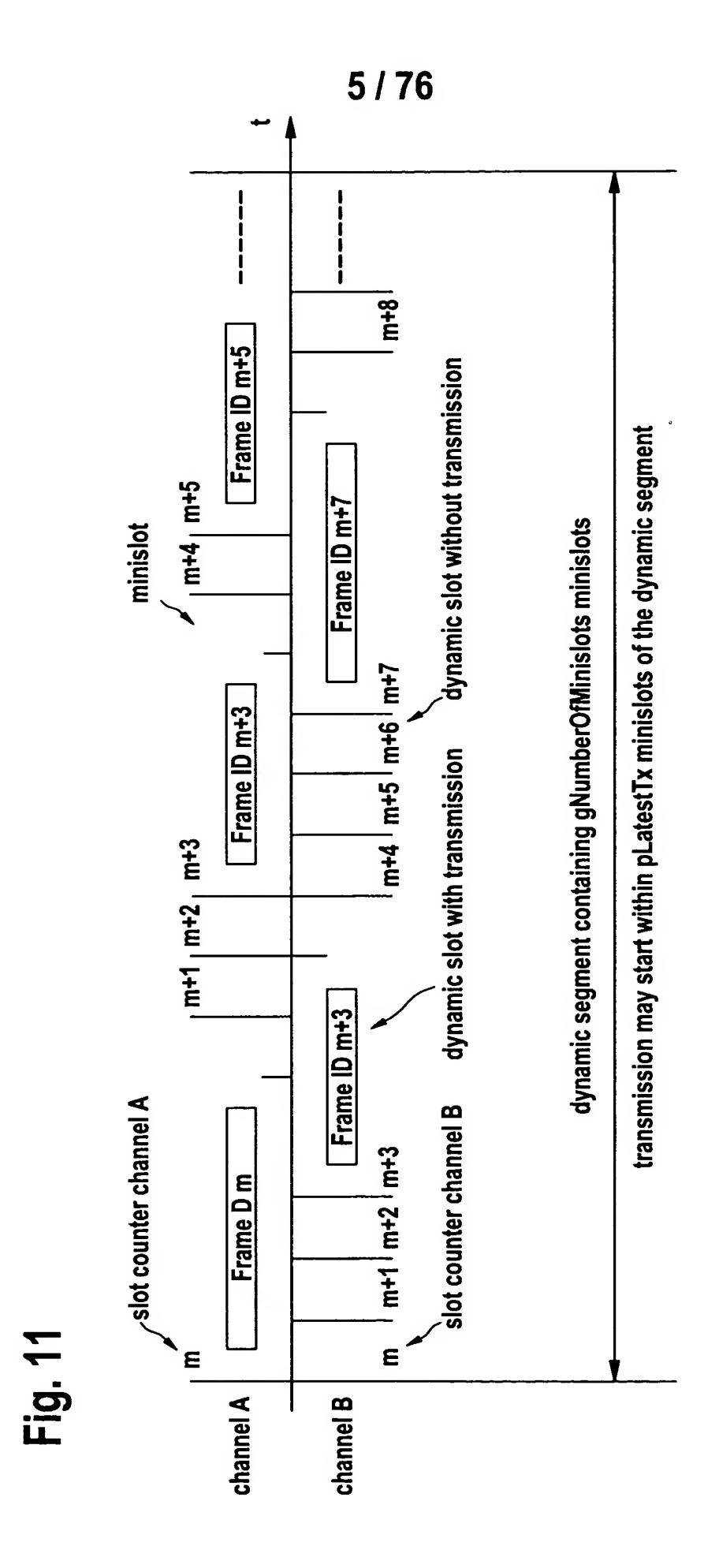
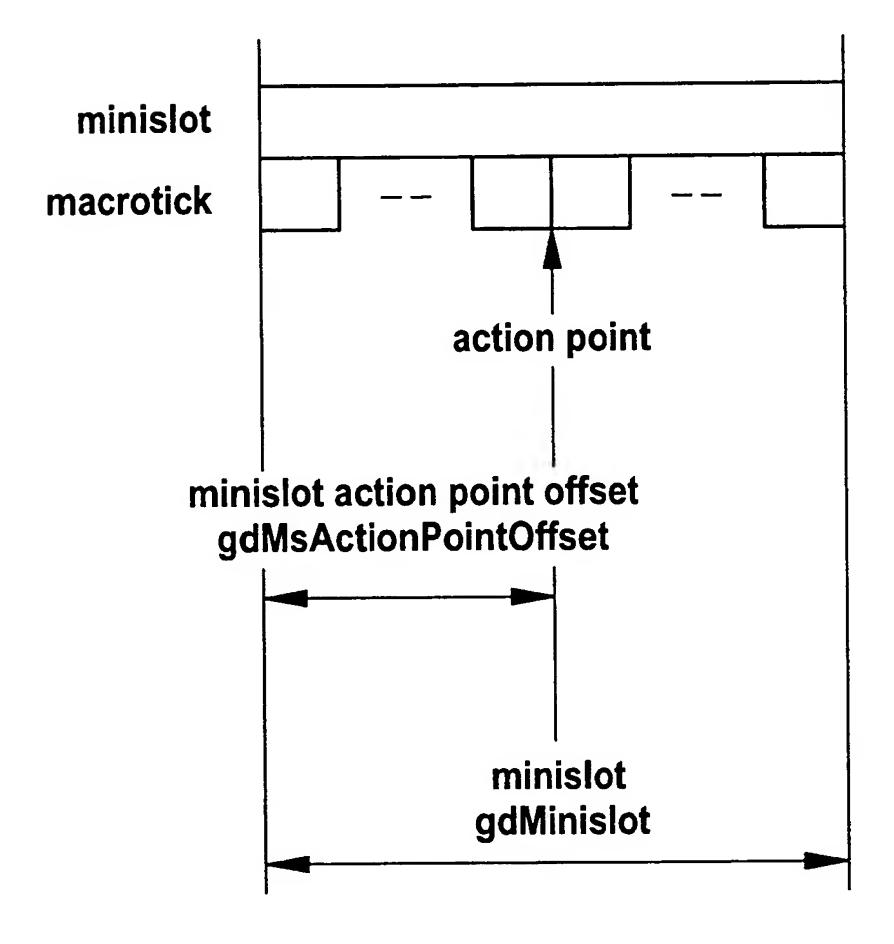
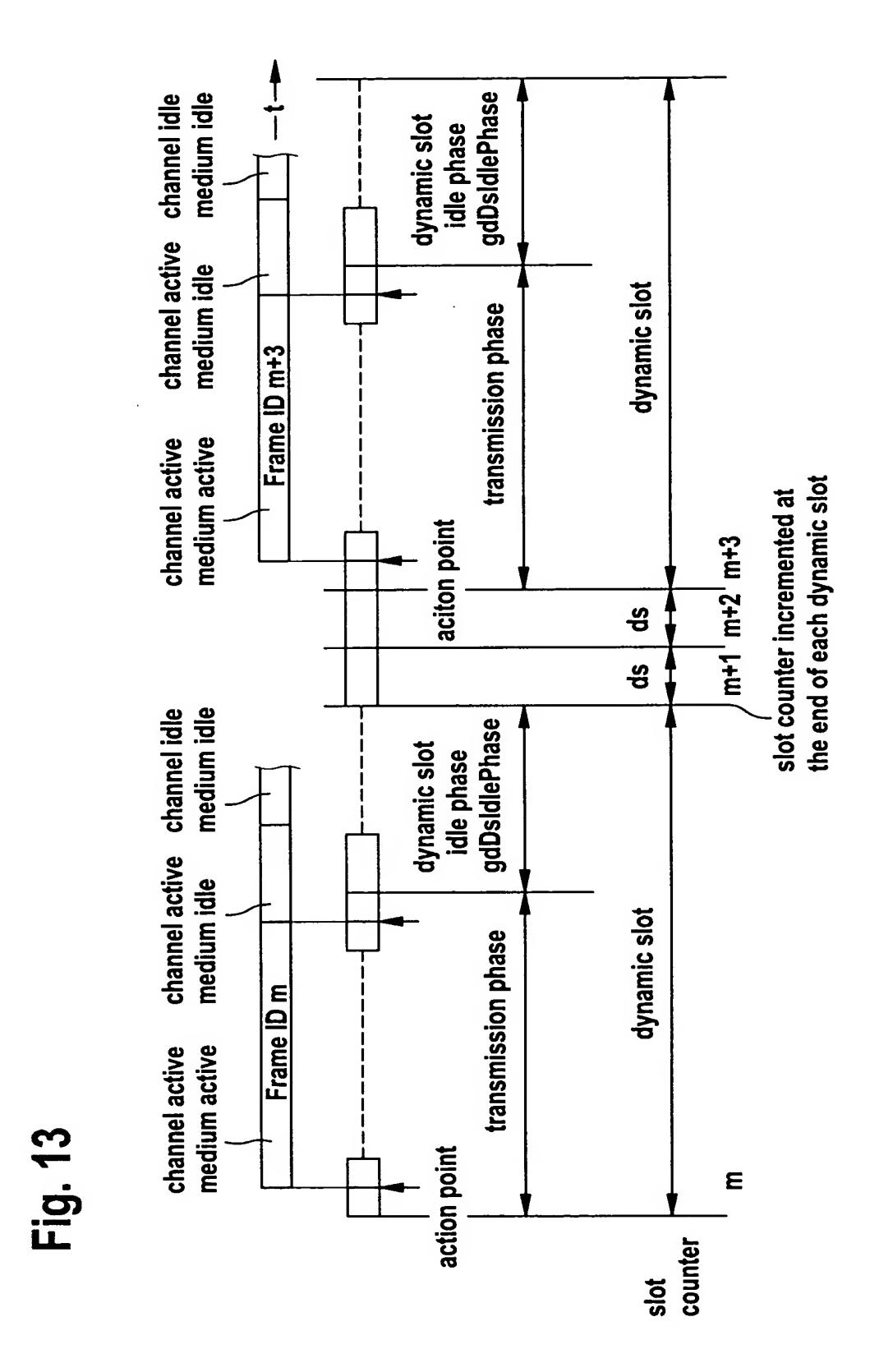


Fig. 12





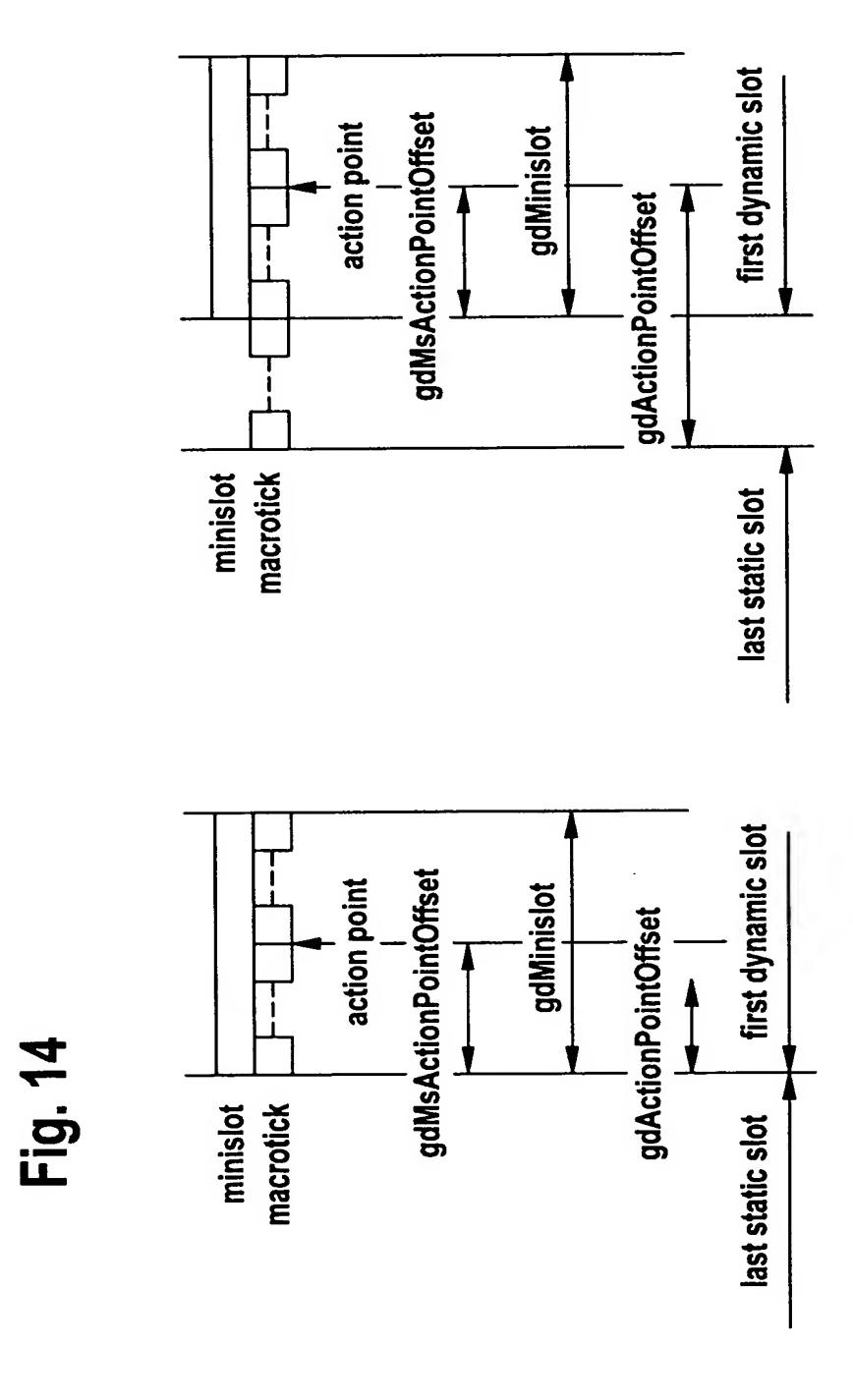


Fig. 15

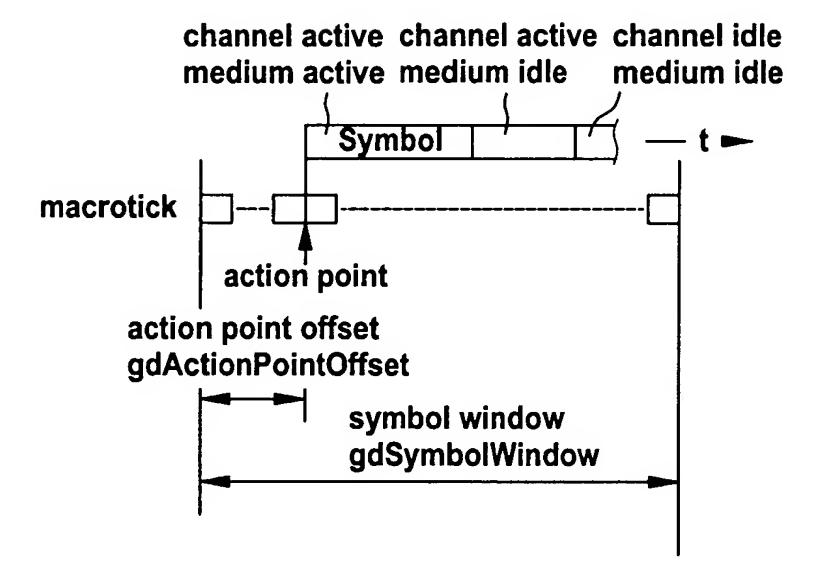
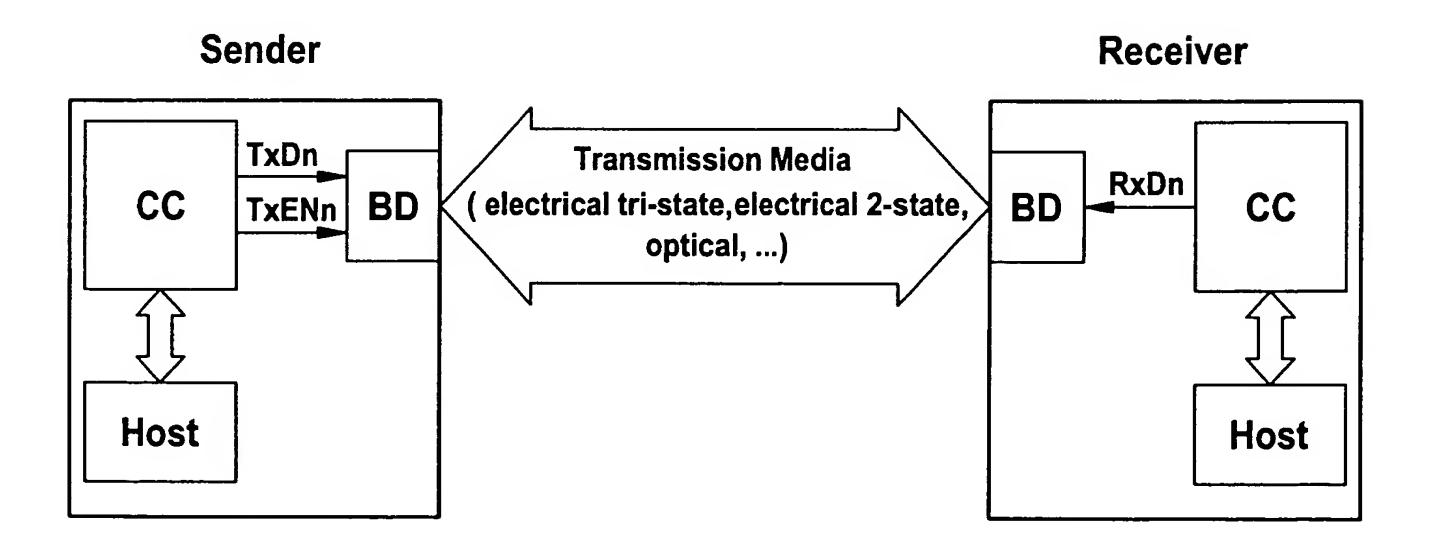
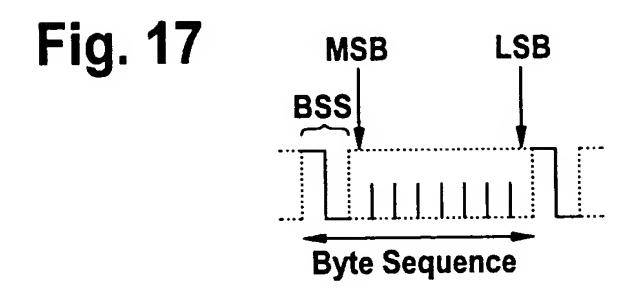
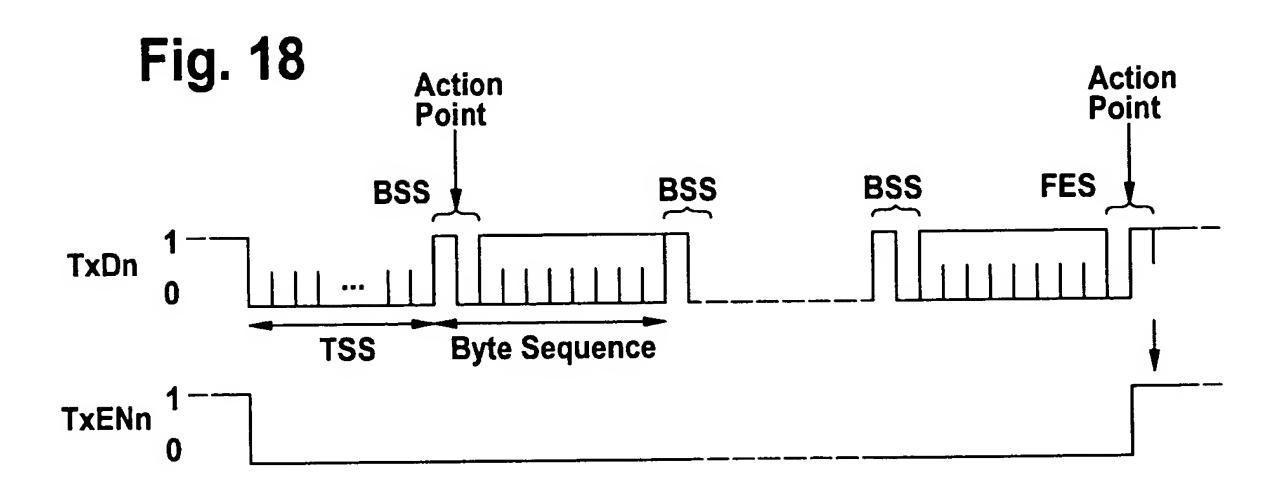
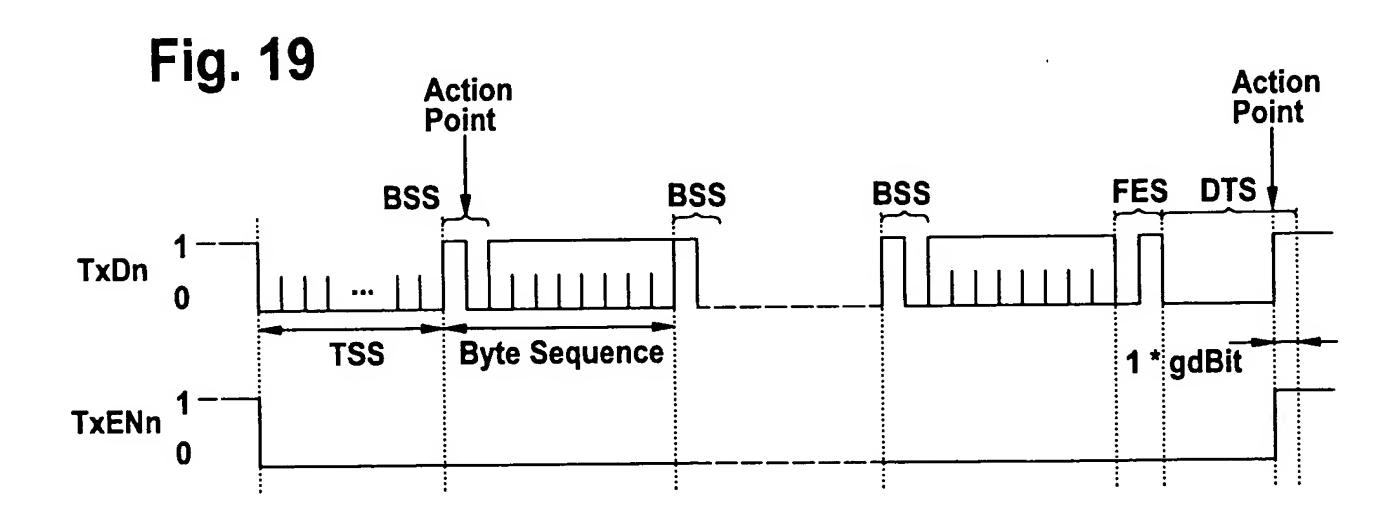


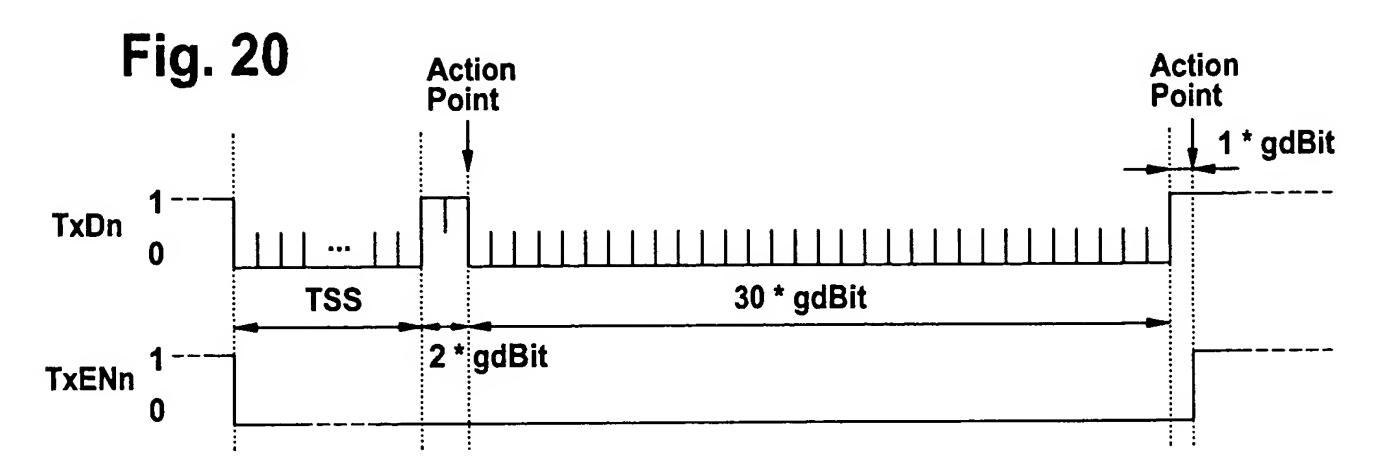
Fig. 16

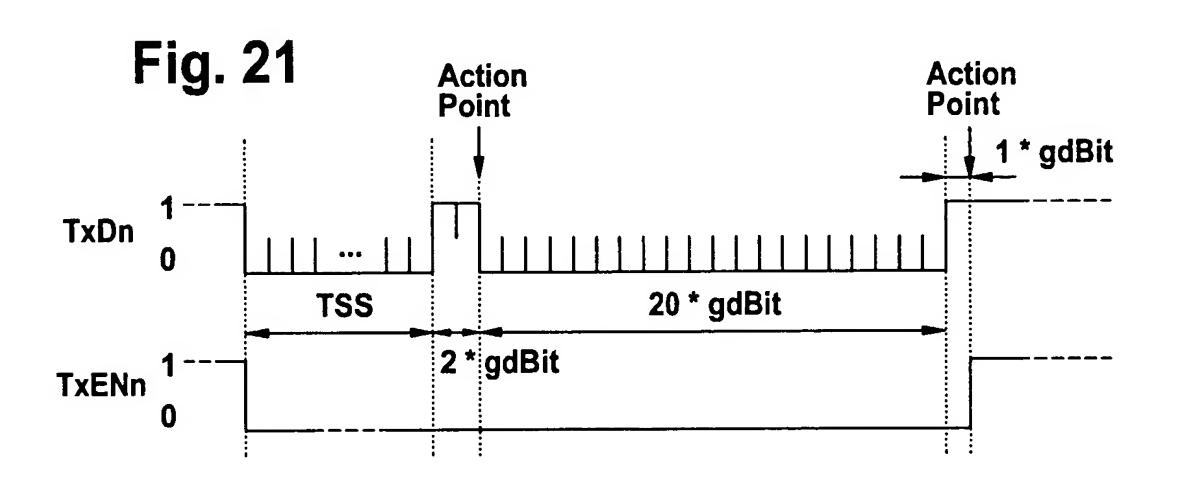












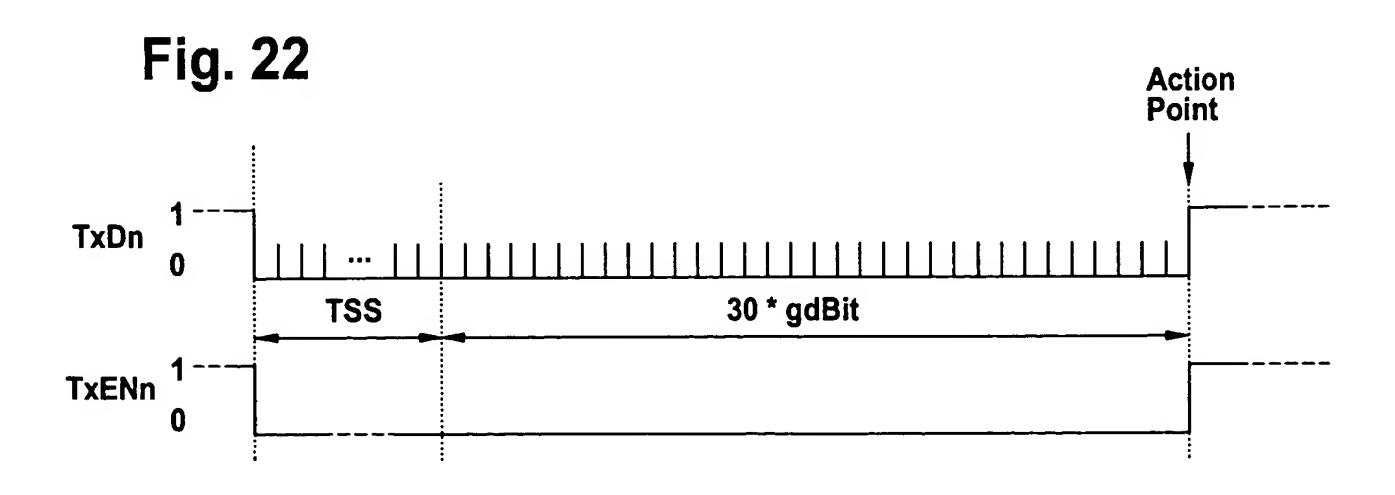


Fig. 23

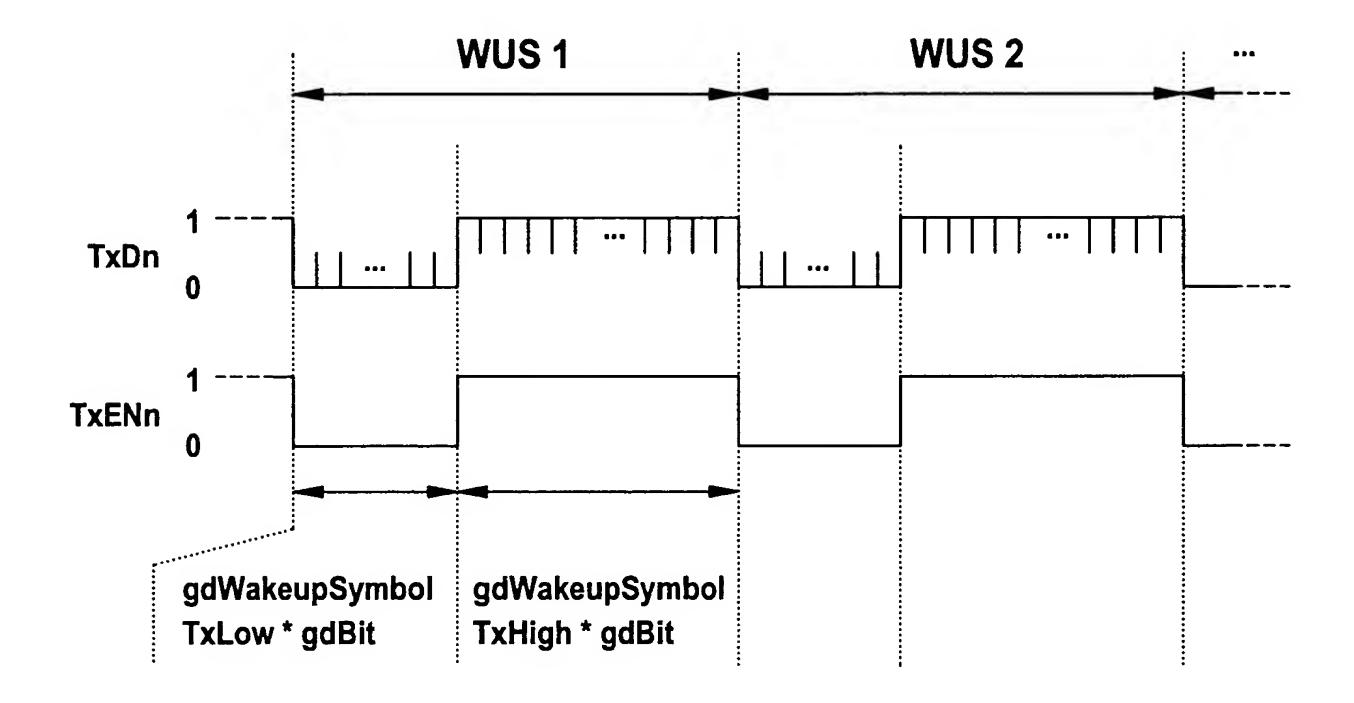


Fig. 24

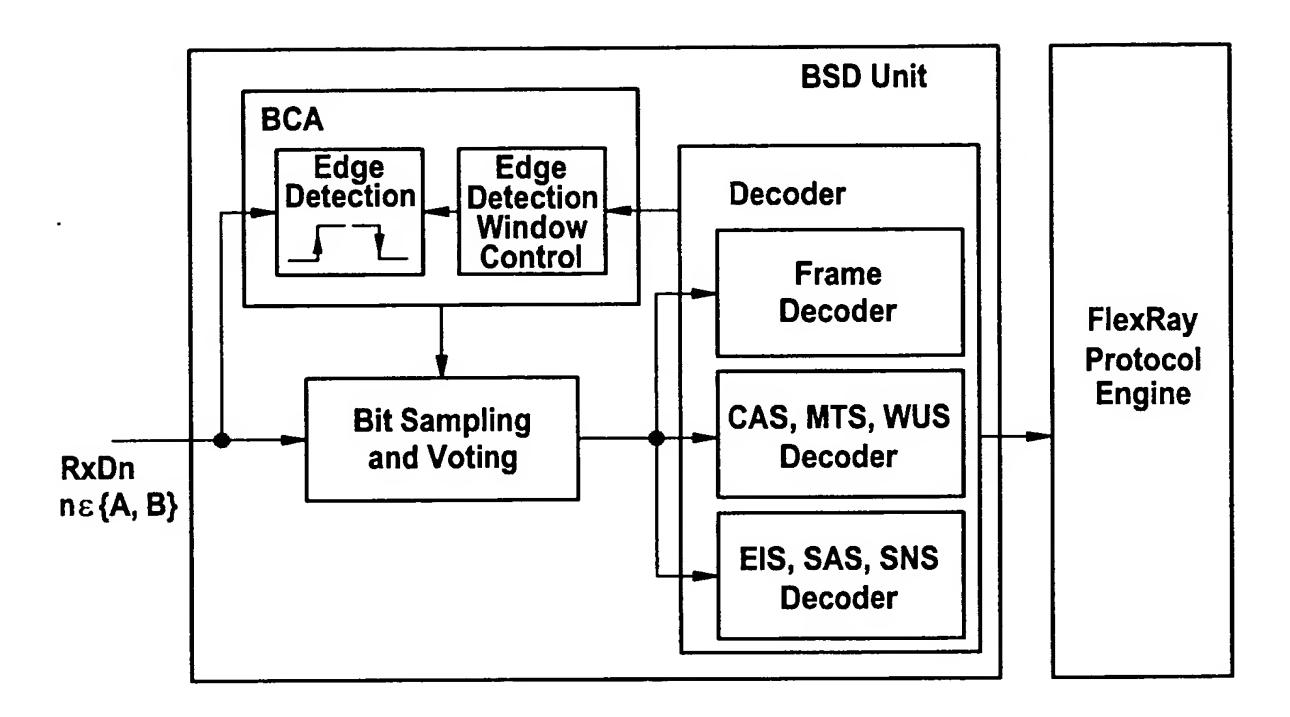


Fig. 25

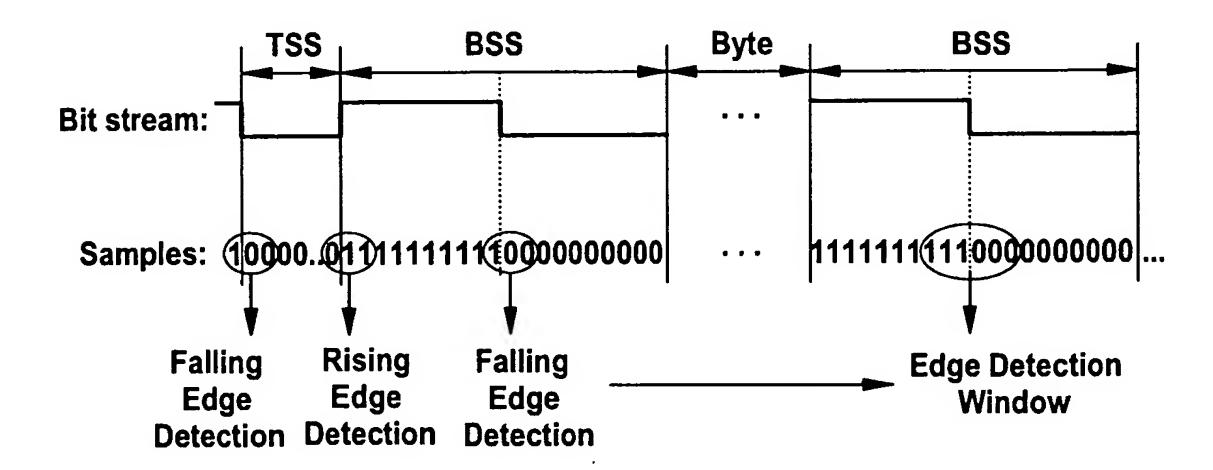


Fig. 26

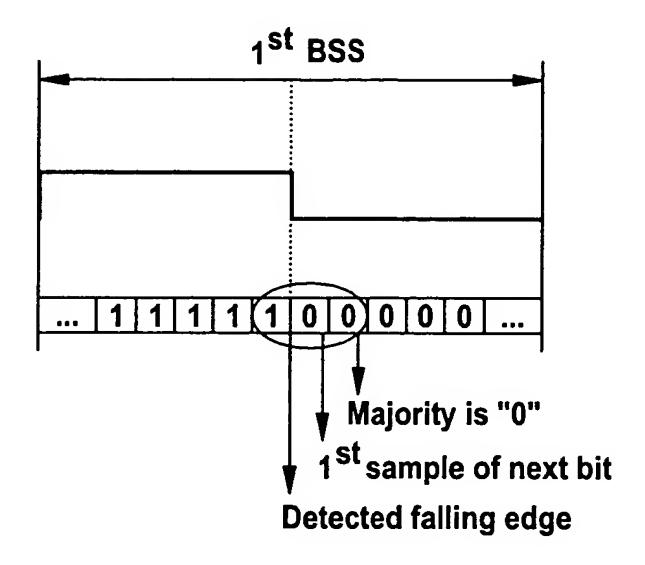


Fig. 27

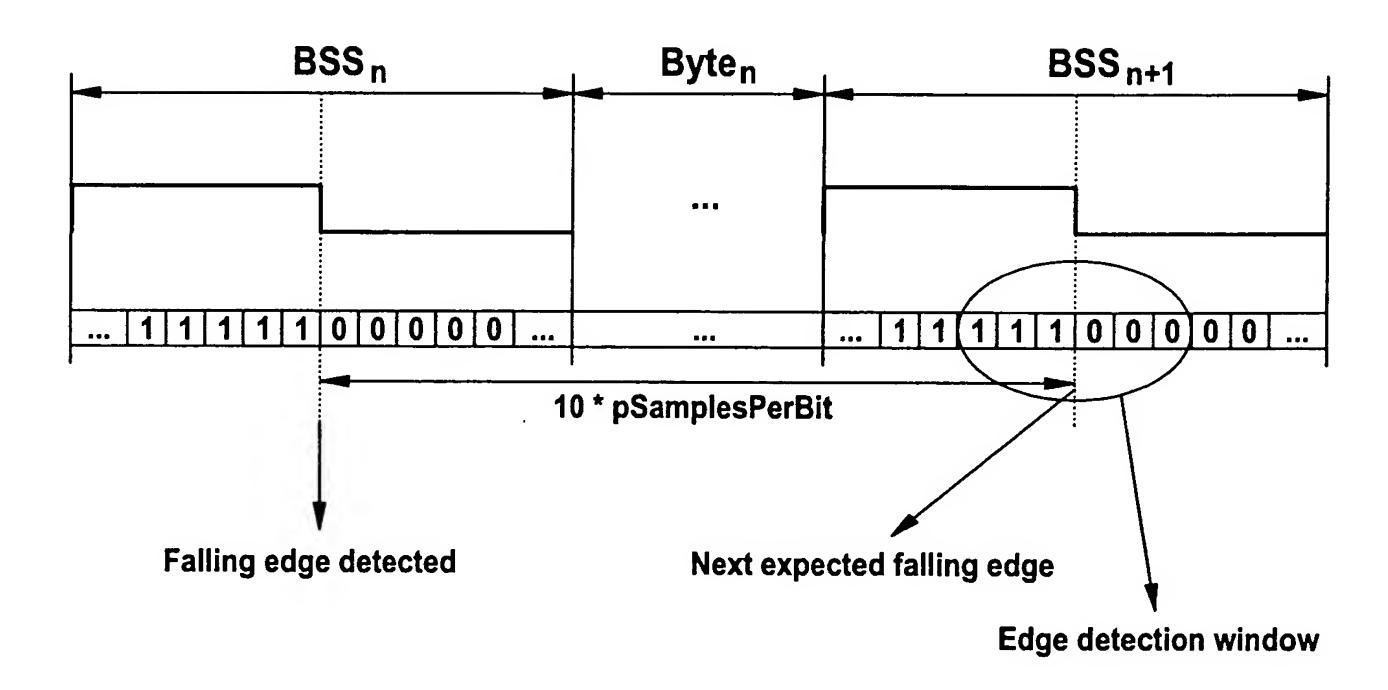


Fig. 28

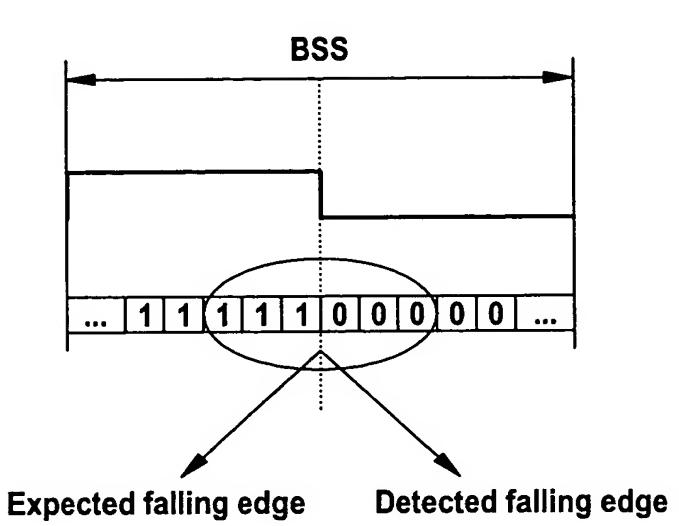


Fig. 29

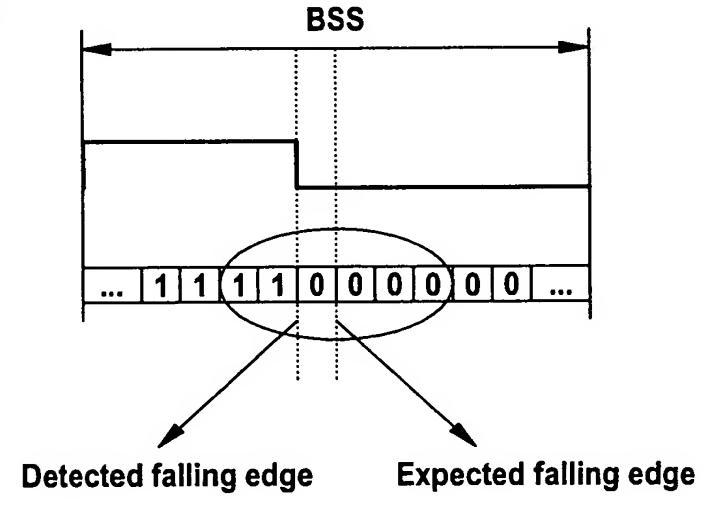


Fig. 30

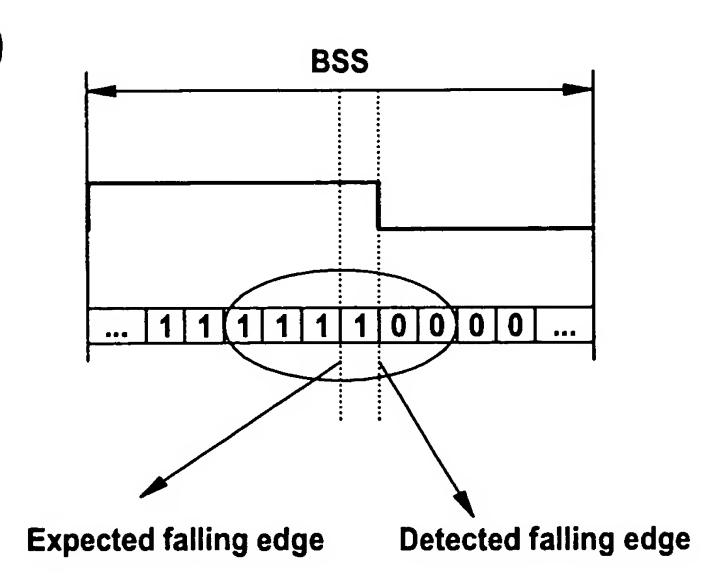
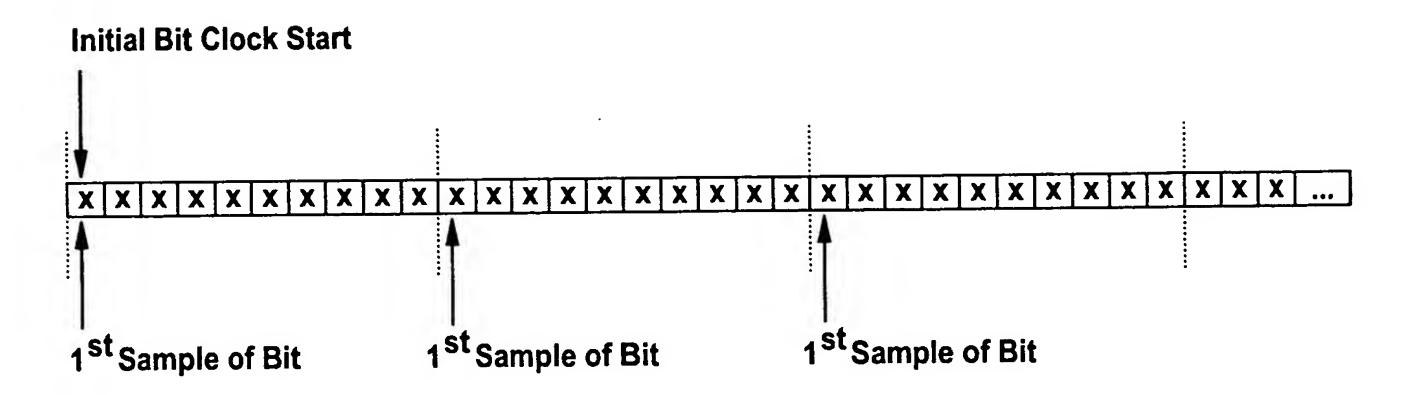


Fig. 31



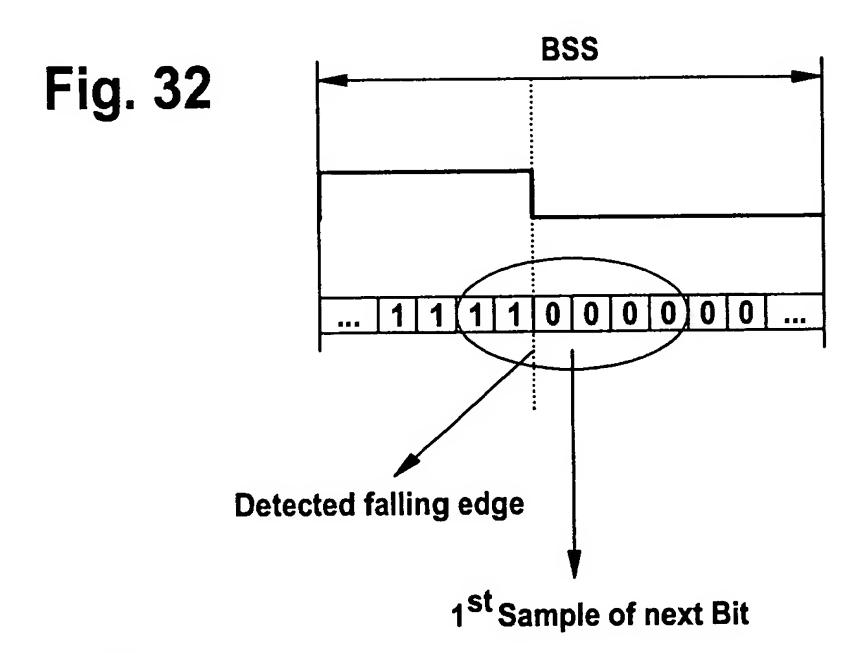


Fig. 33

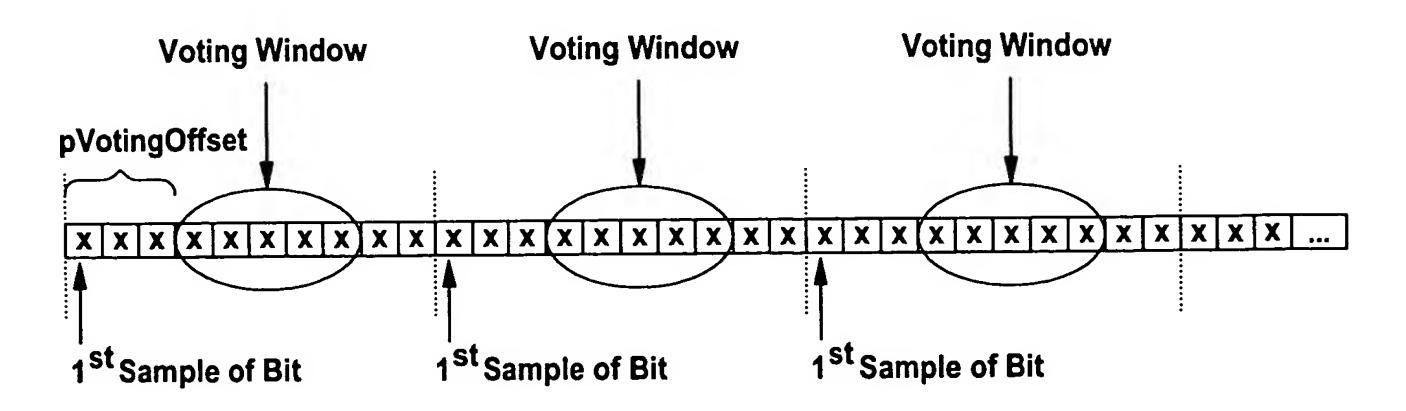


Fig. 34

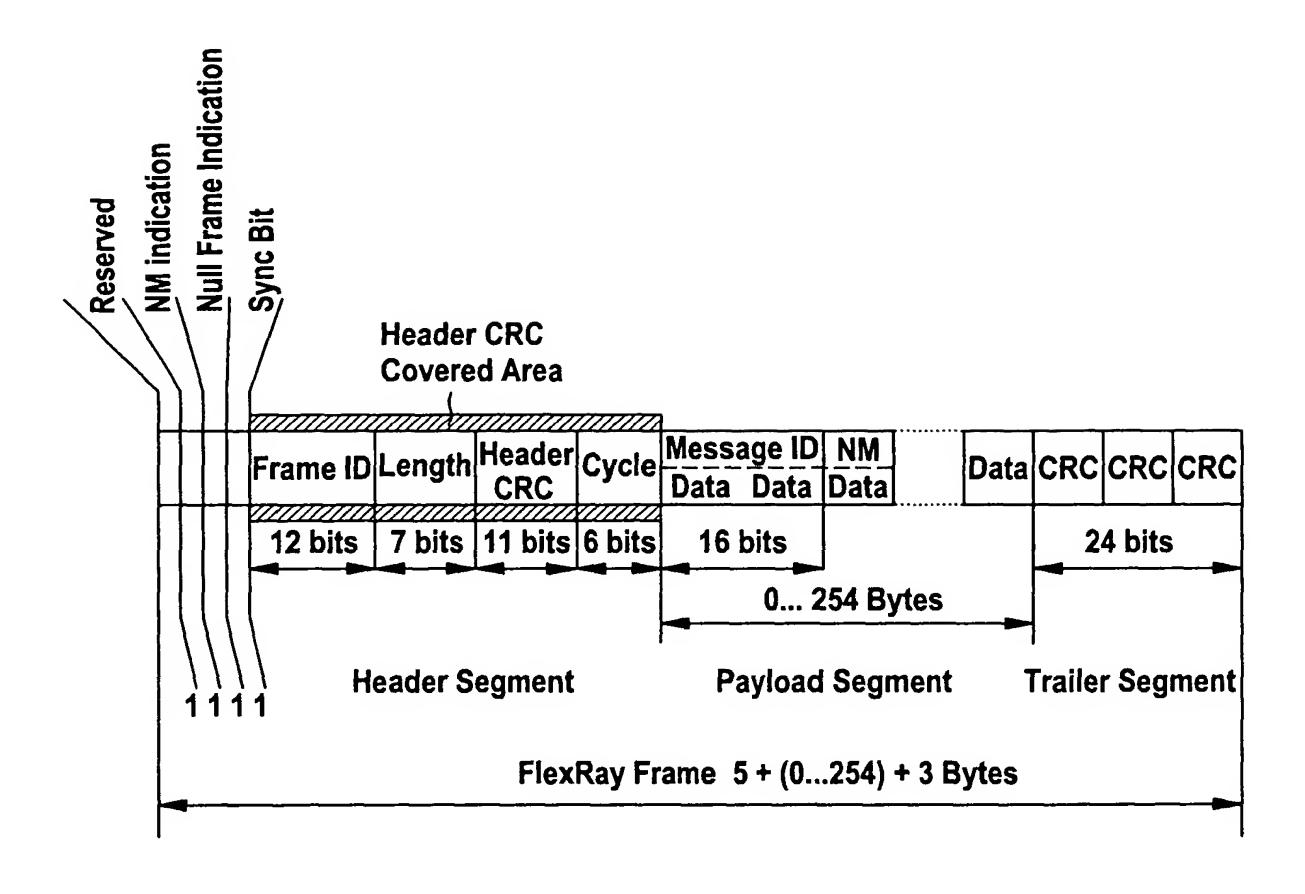


Fig. 35

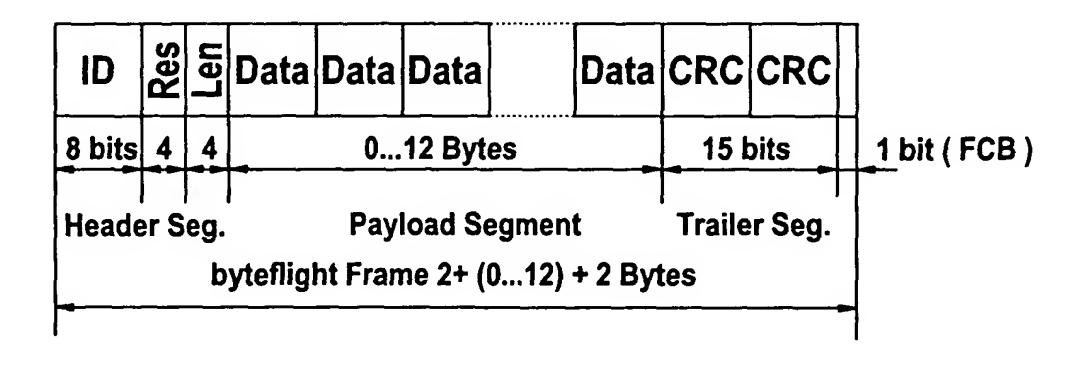


Fig. 36

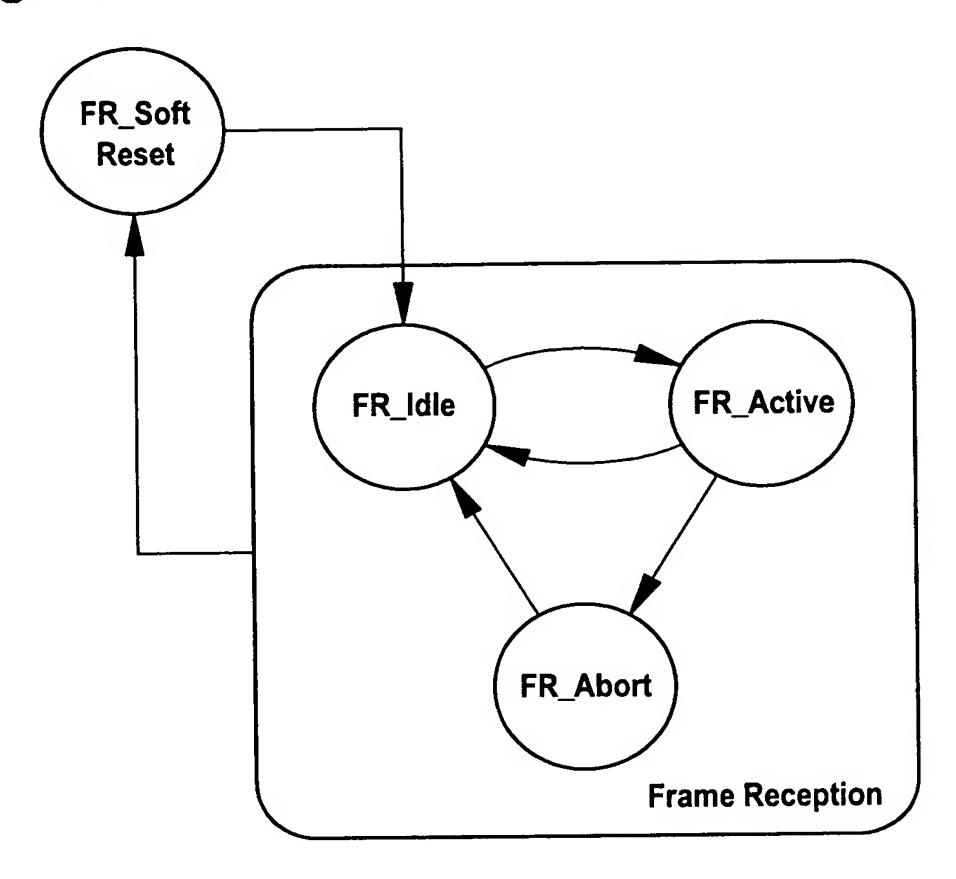


Fig. 37

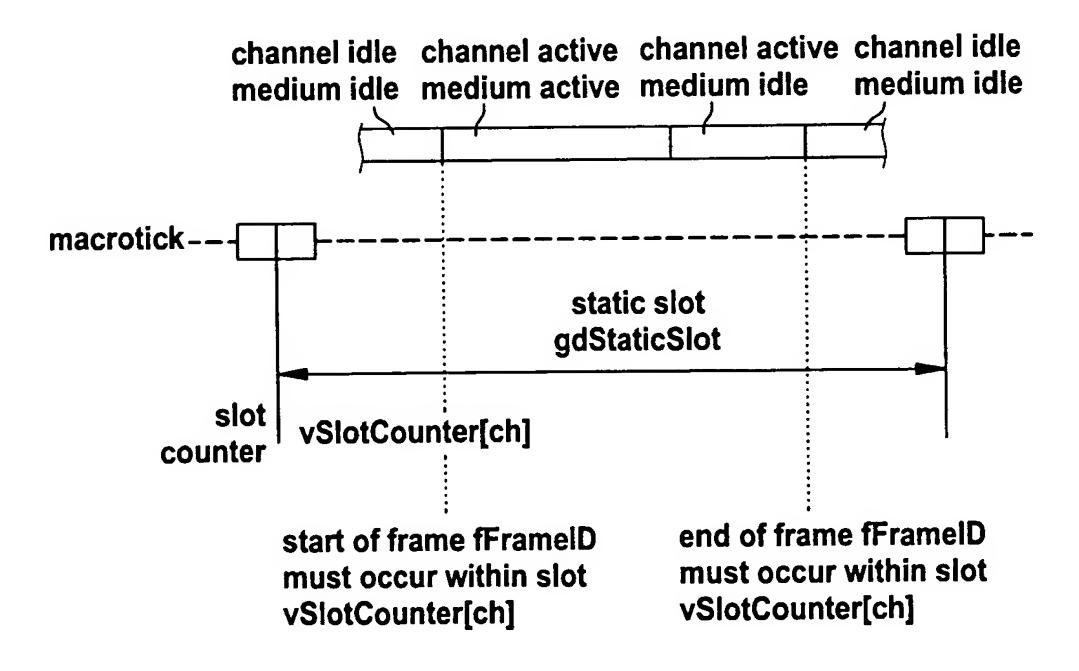


Fig. 38

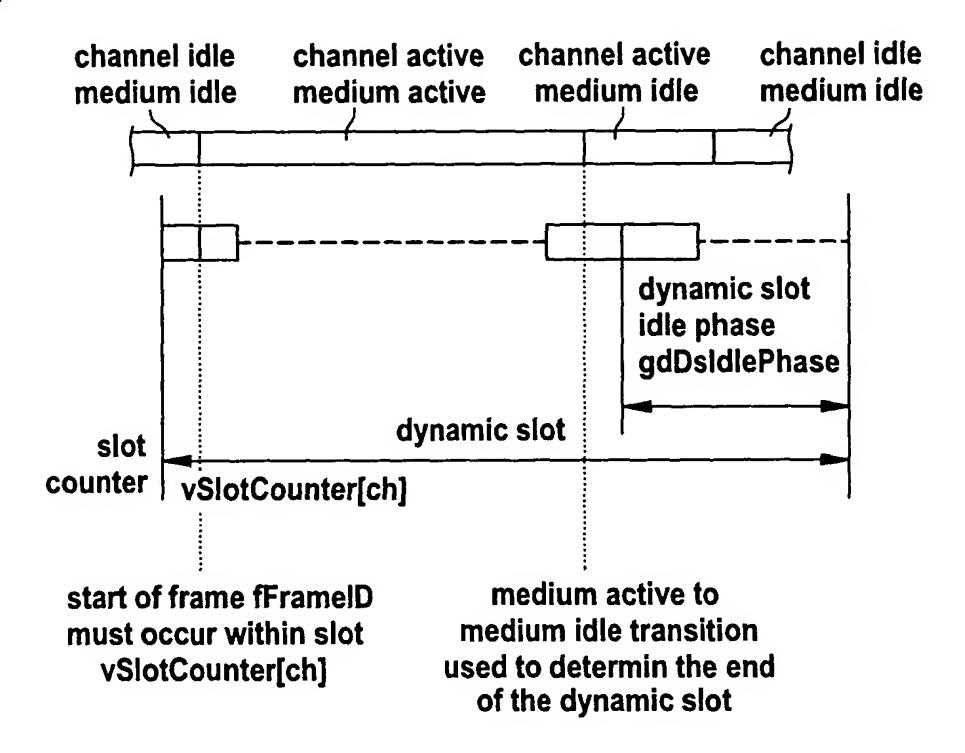
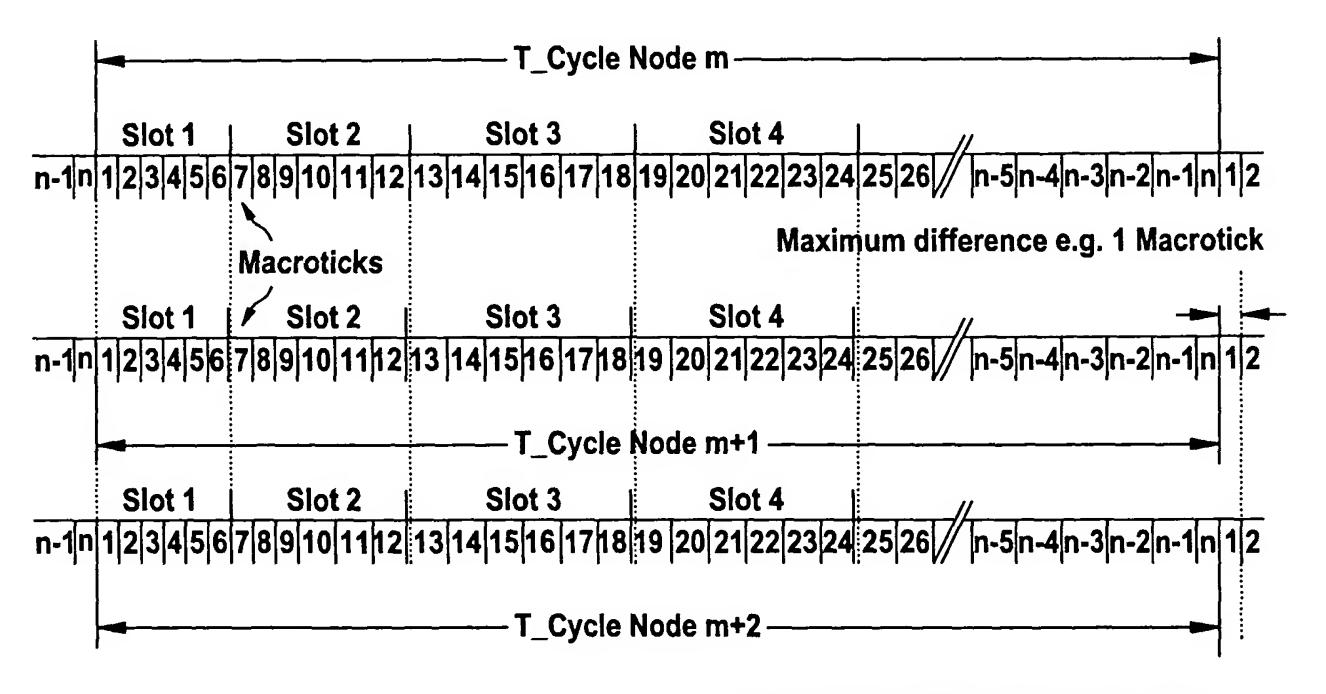


Fig. 39



n = number of Macroticks per cycle

Fig. 40

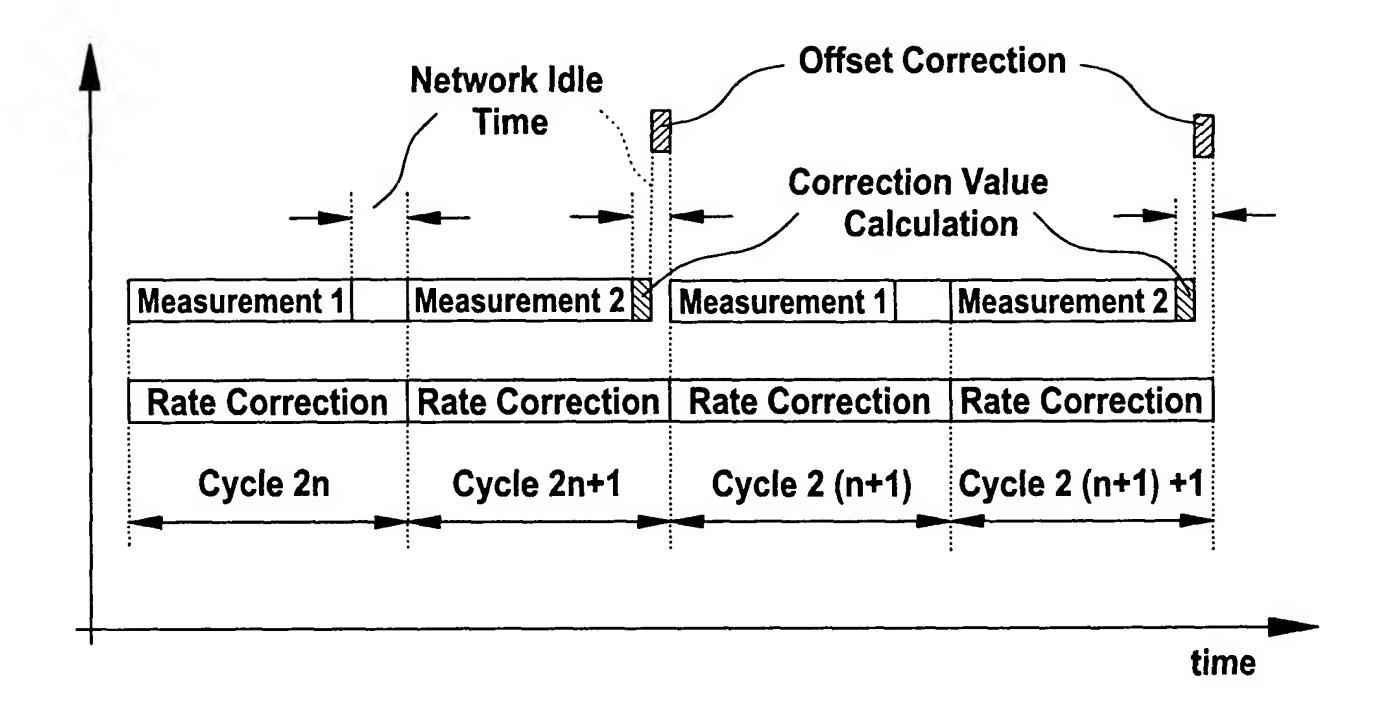


Fig. 41

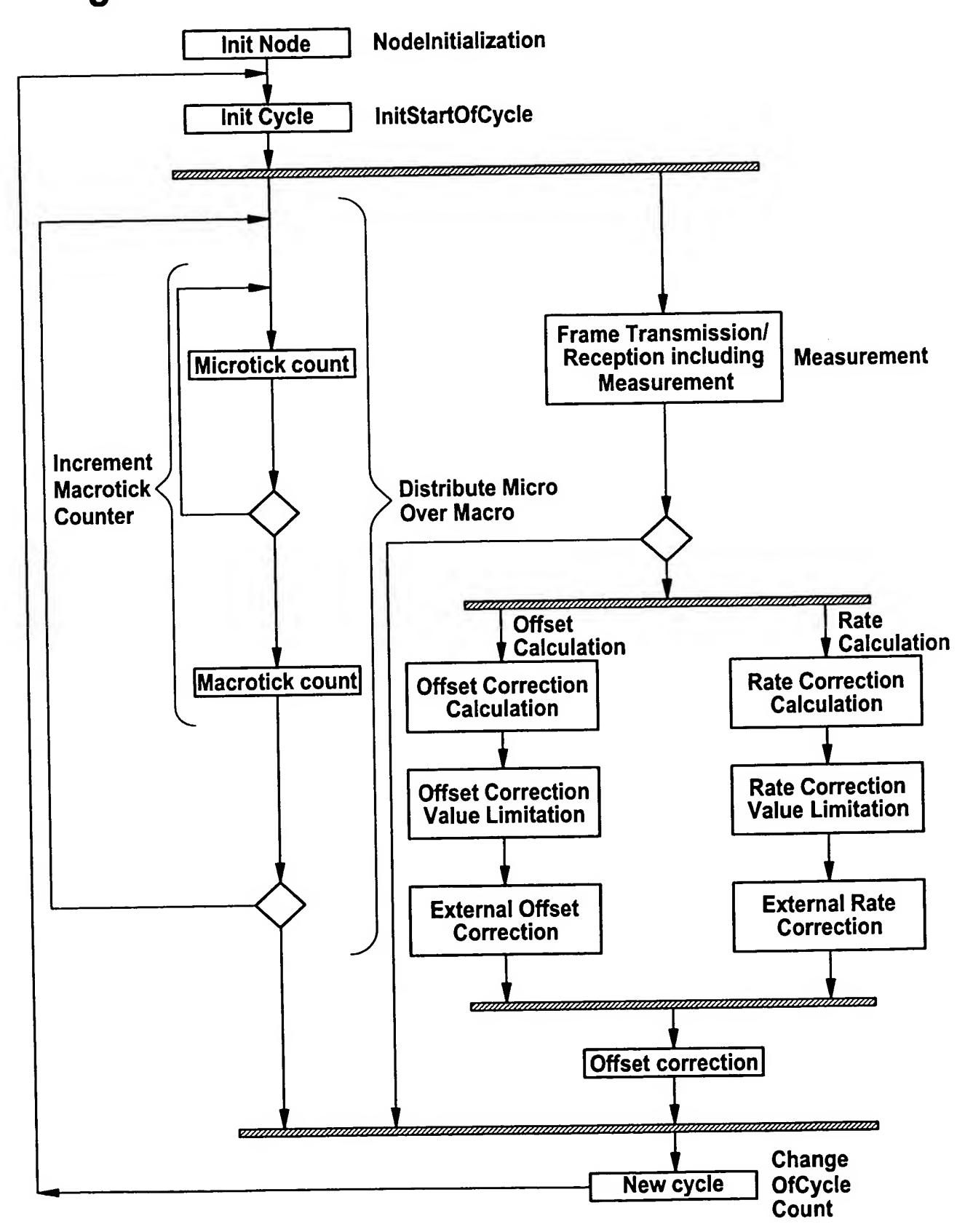
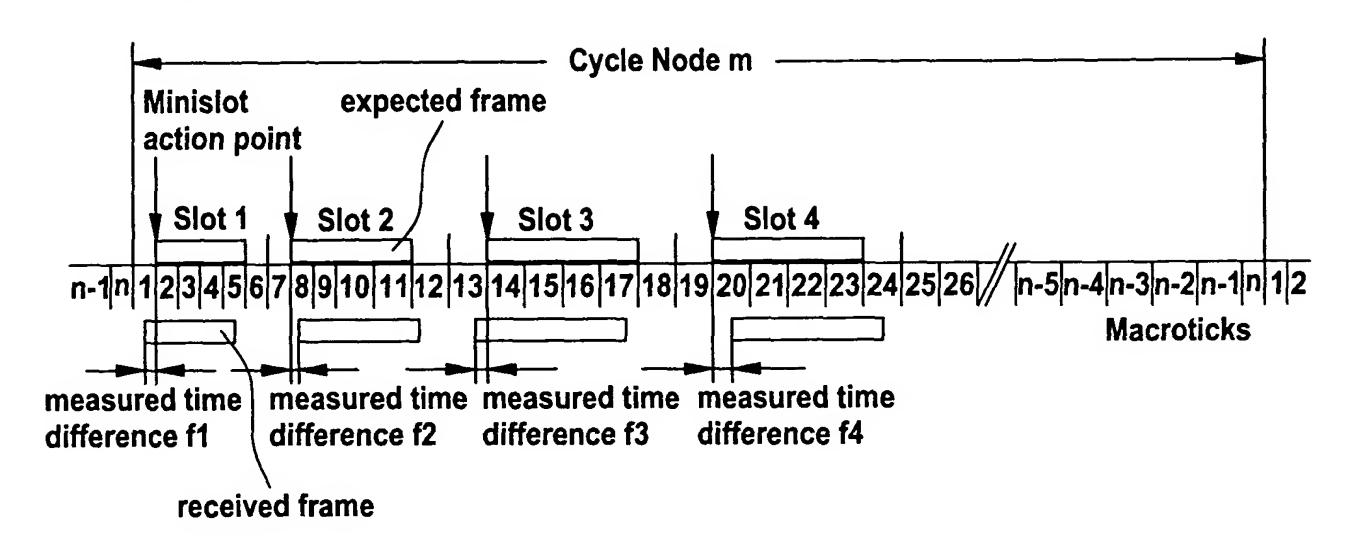


Fig. 42



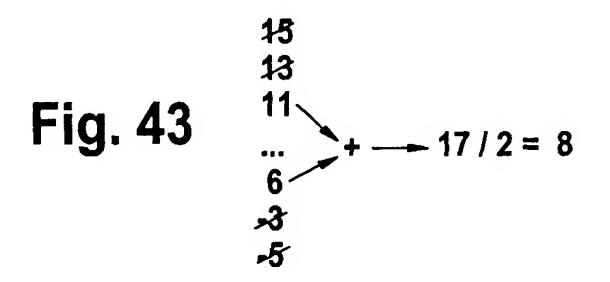


Fig. 44

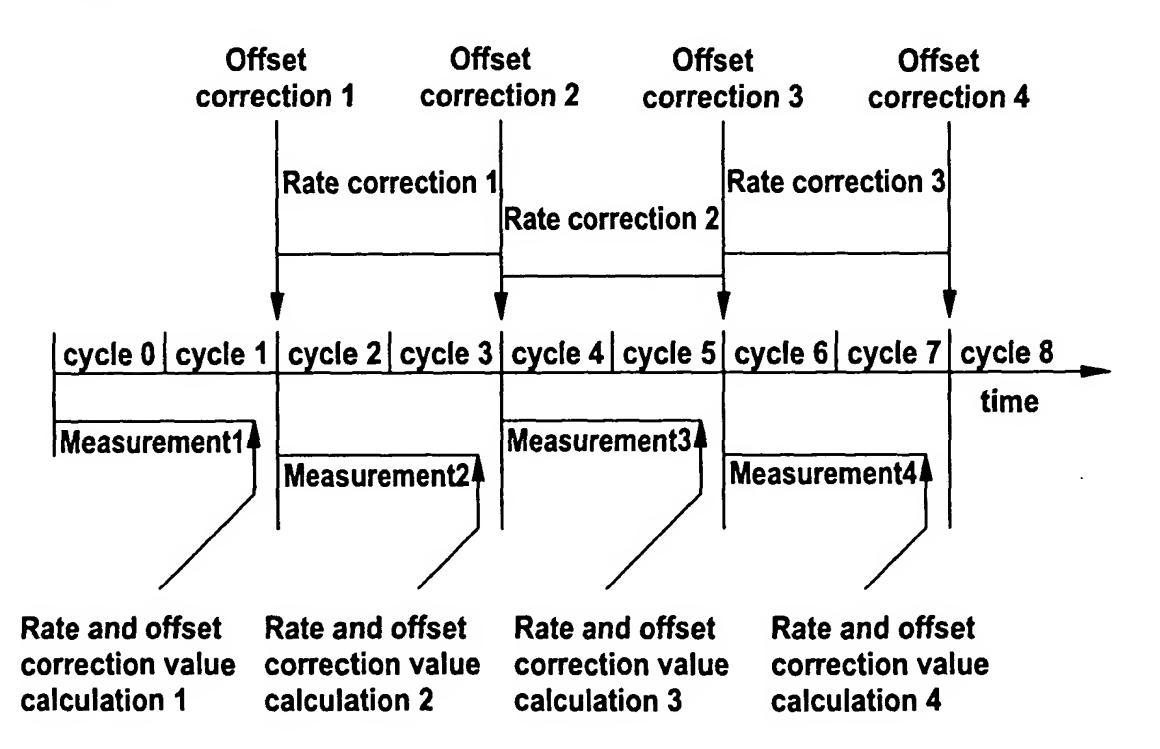


Fig. 45

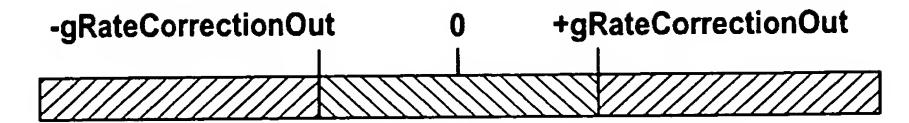
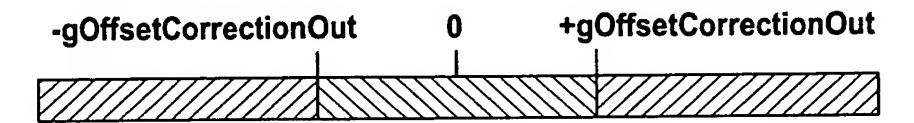


Fig. 46



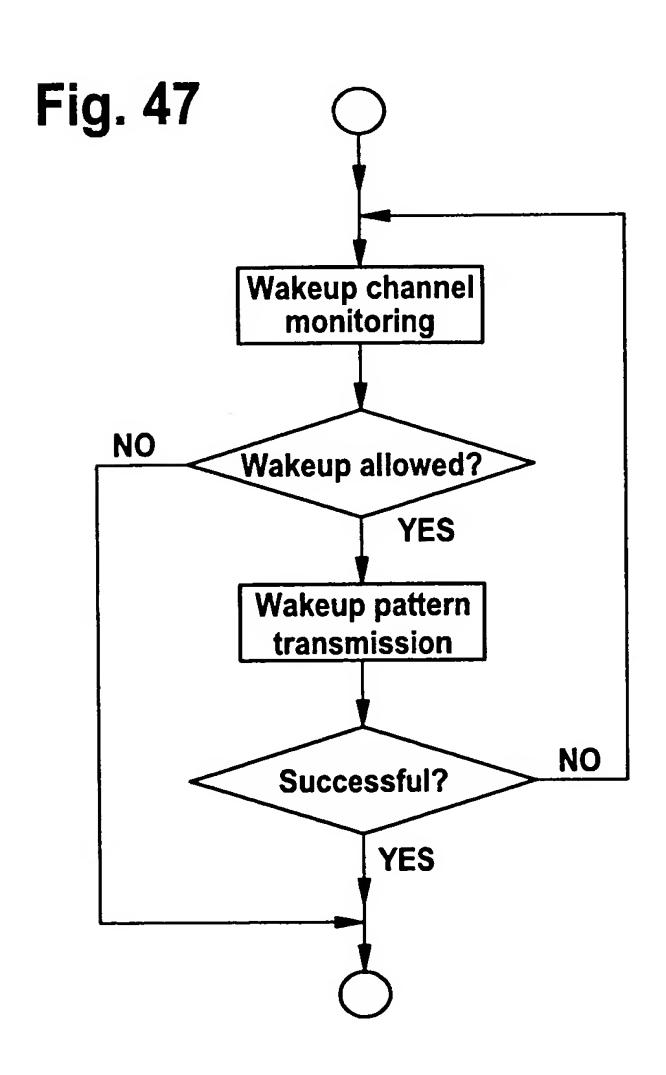


Fig. 48

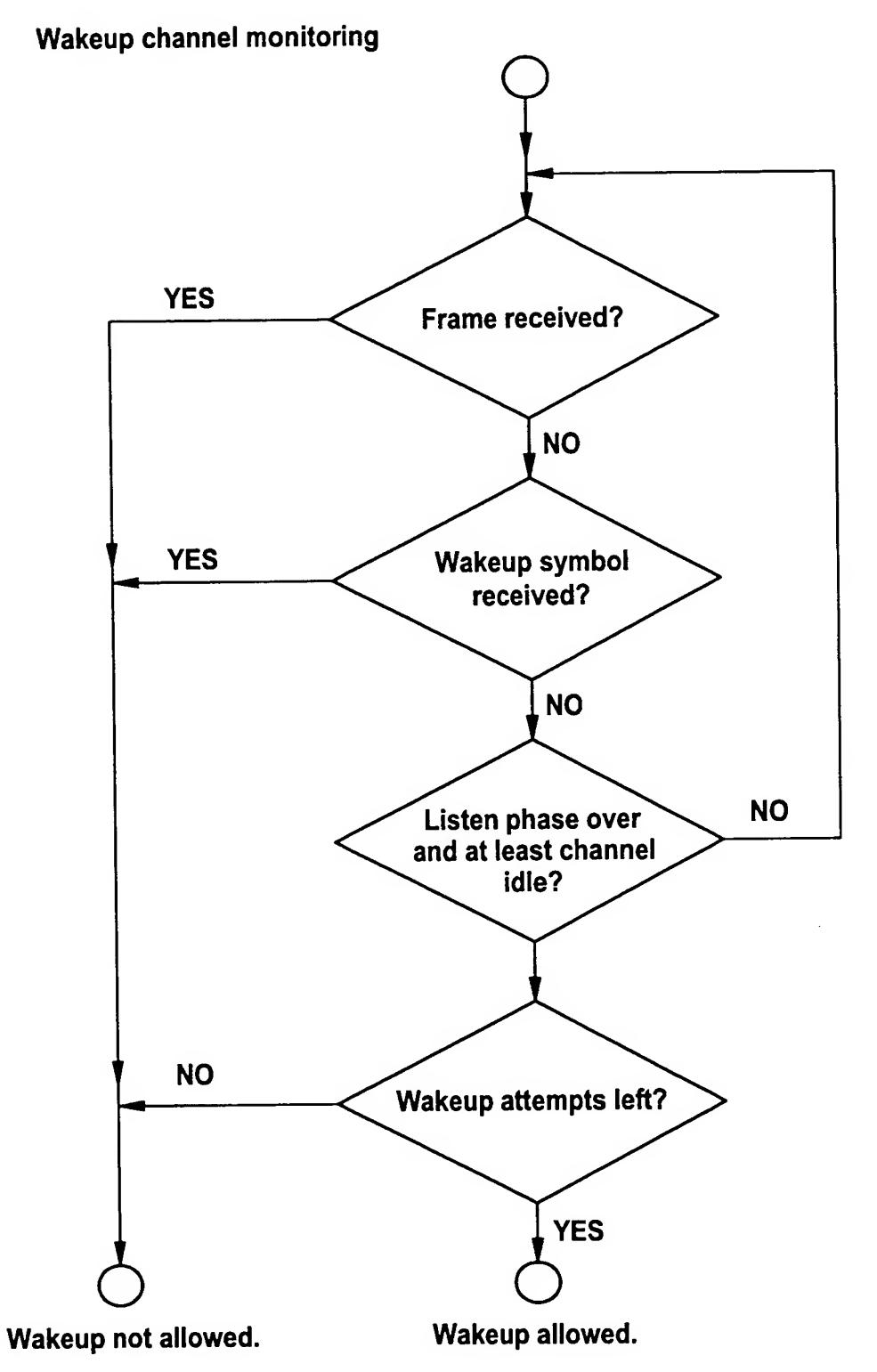


Fig. 49
Wakeup pattern transmission

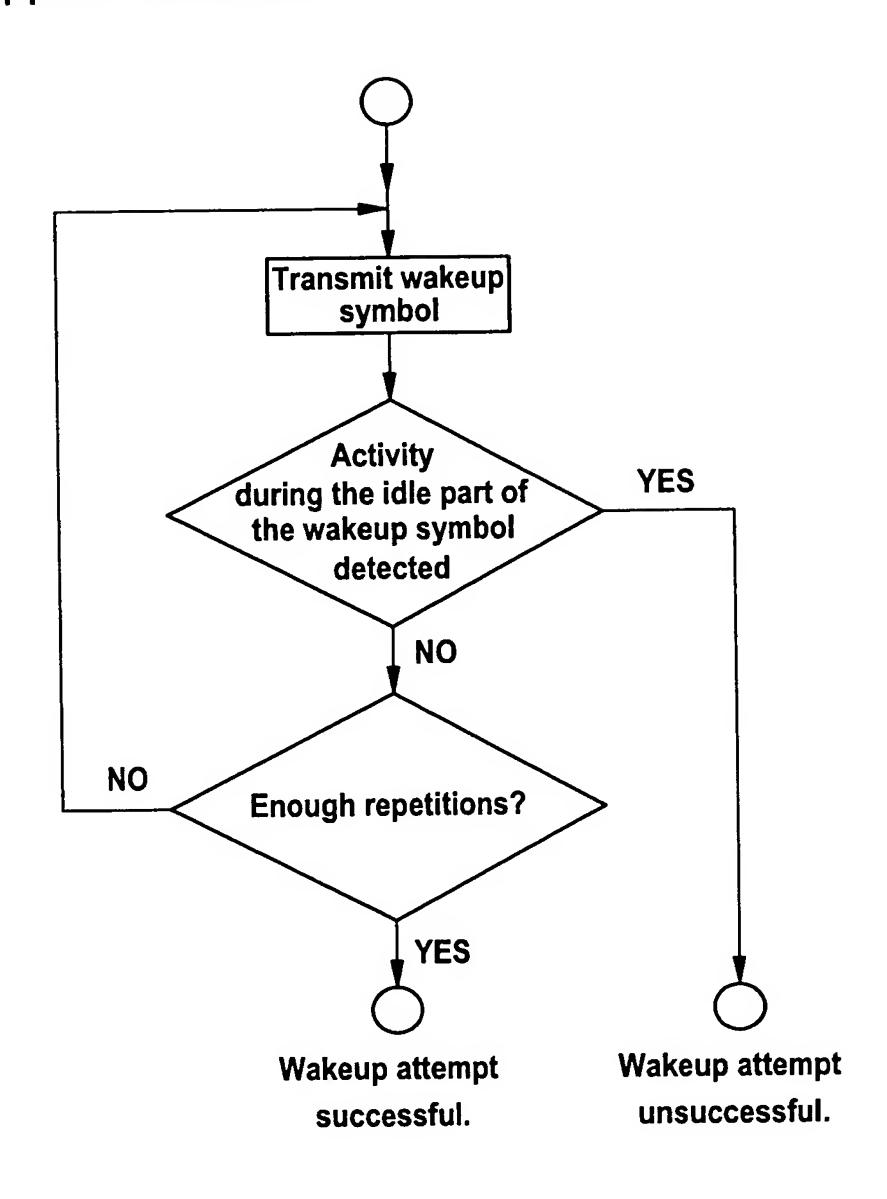


Fig. 50

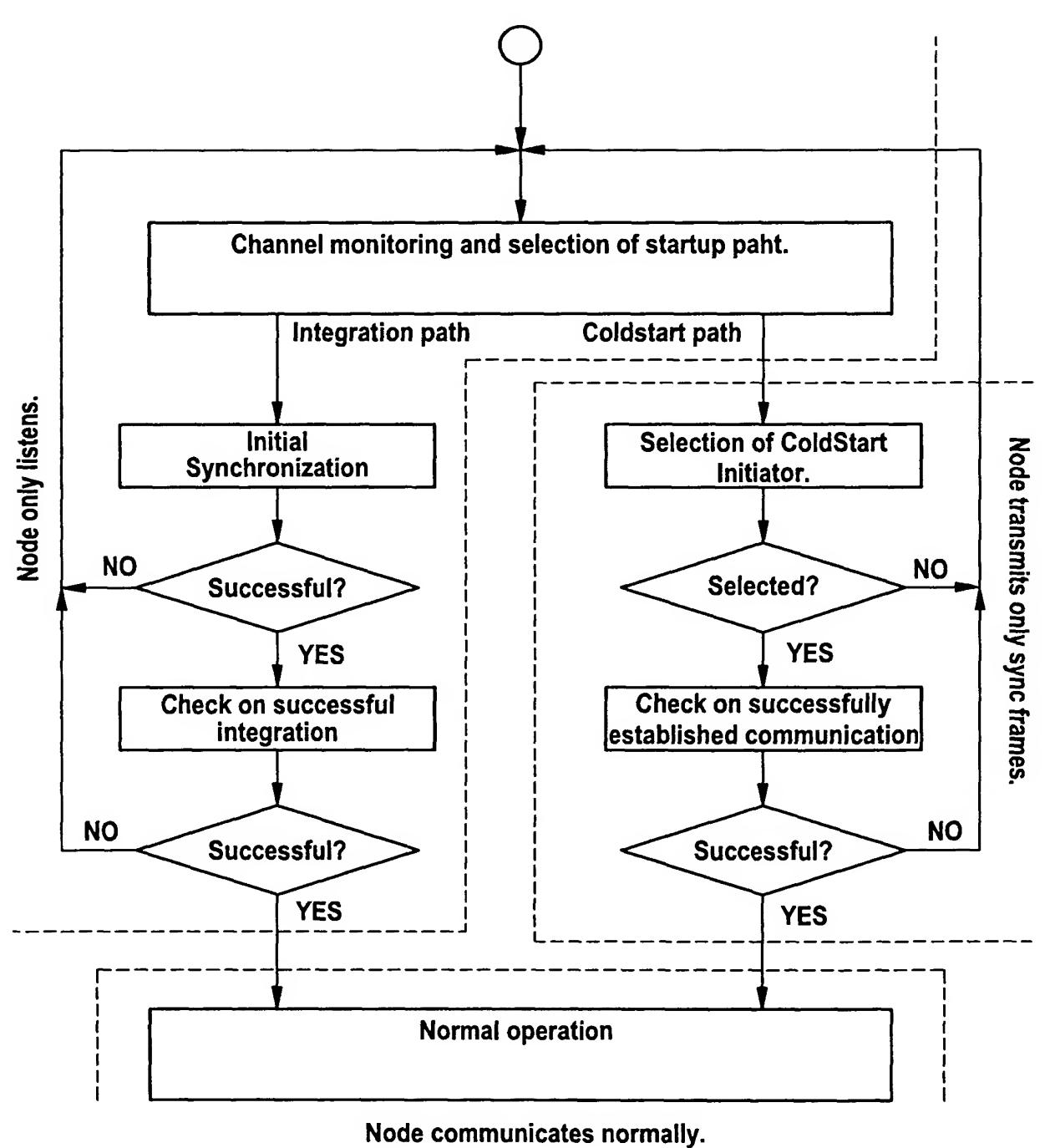


Fig. 51
Channel monitoring and selection of startup path.

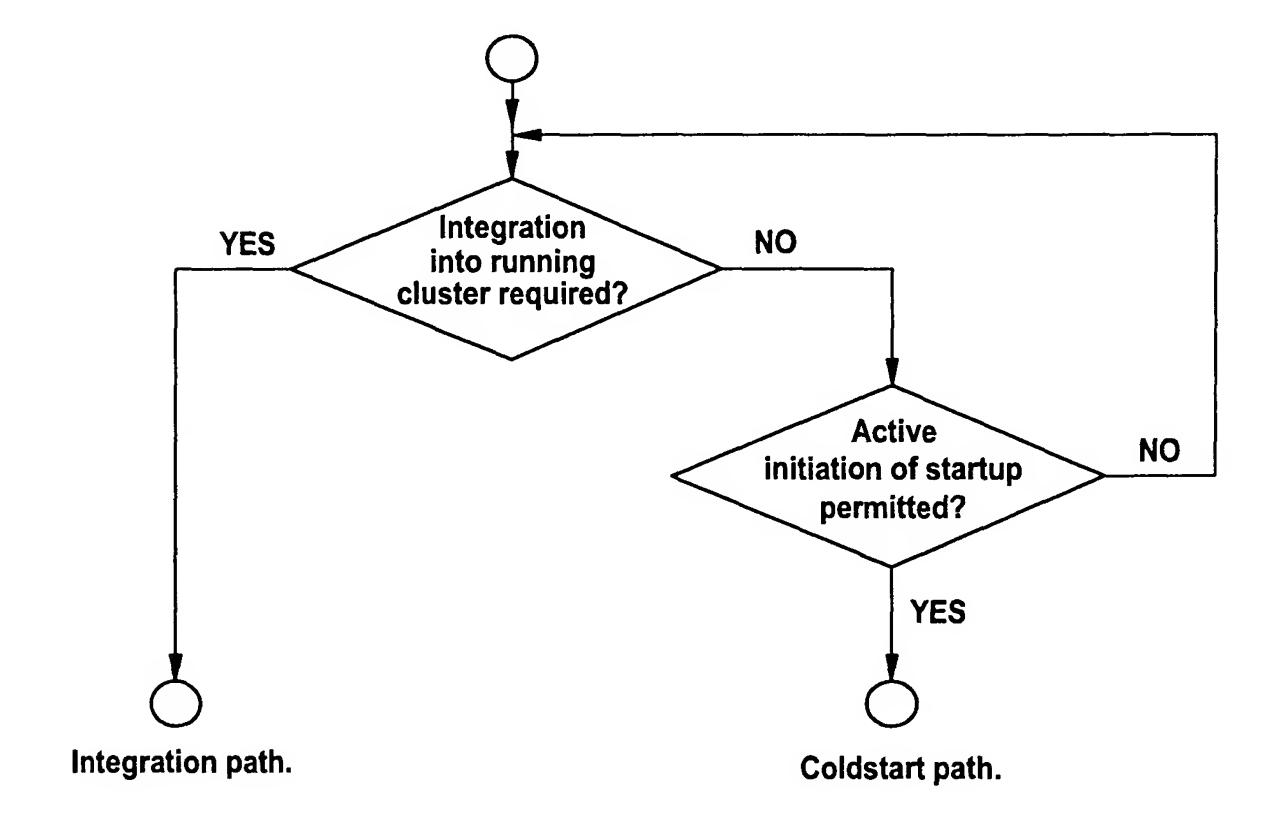


Fig. 52
Selection of ColdStart Initiator

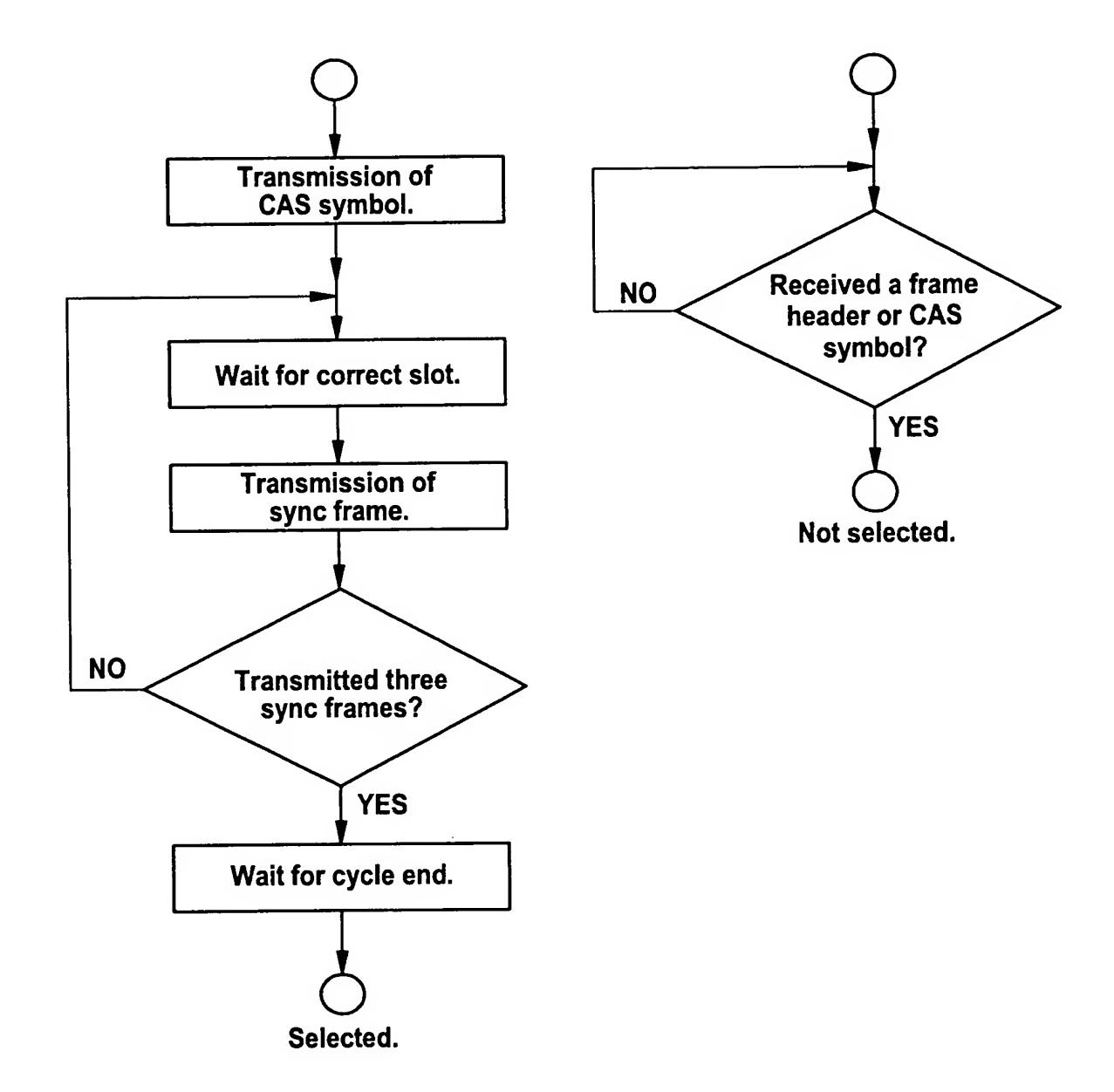


Fig. 53
Check on successfully established communication

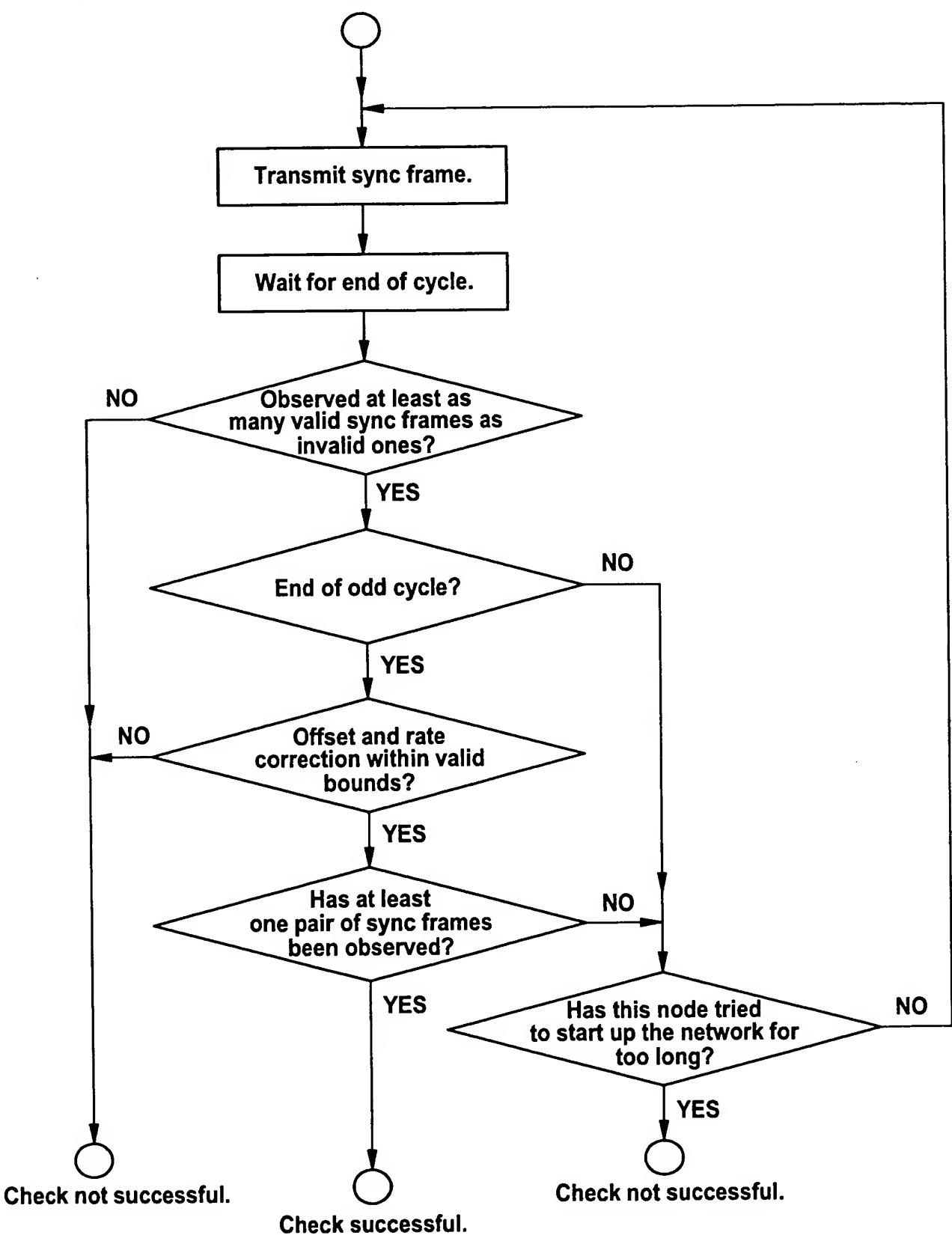


Fig. 54
Initial Synchronization

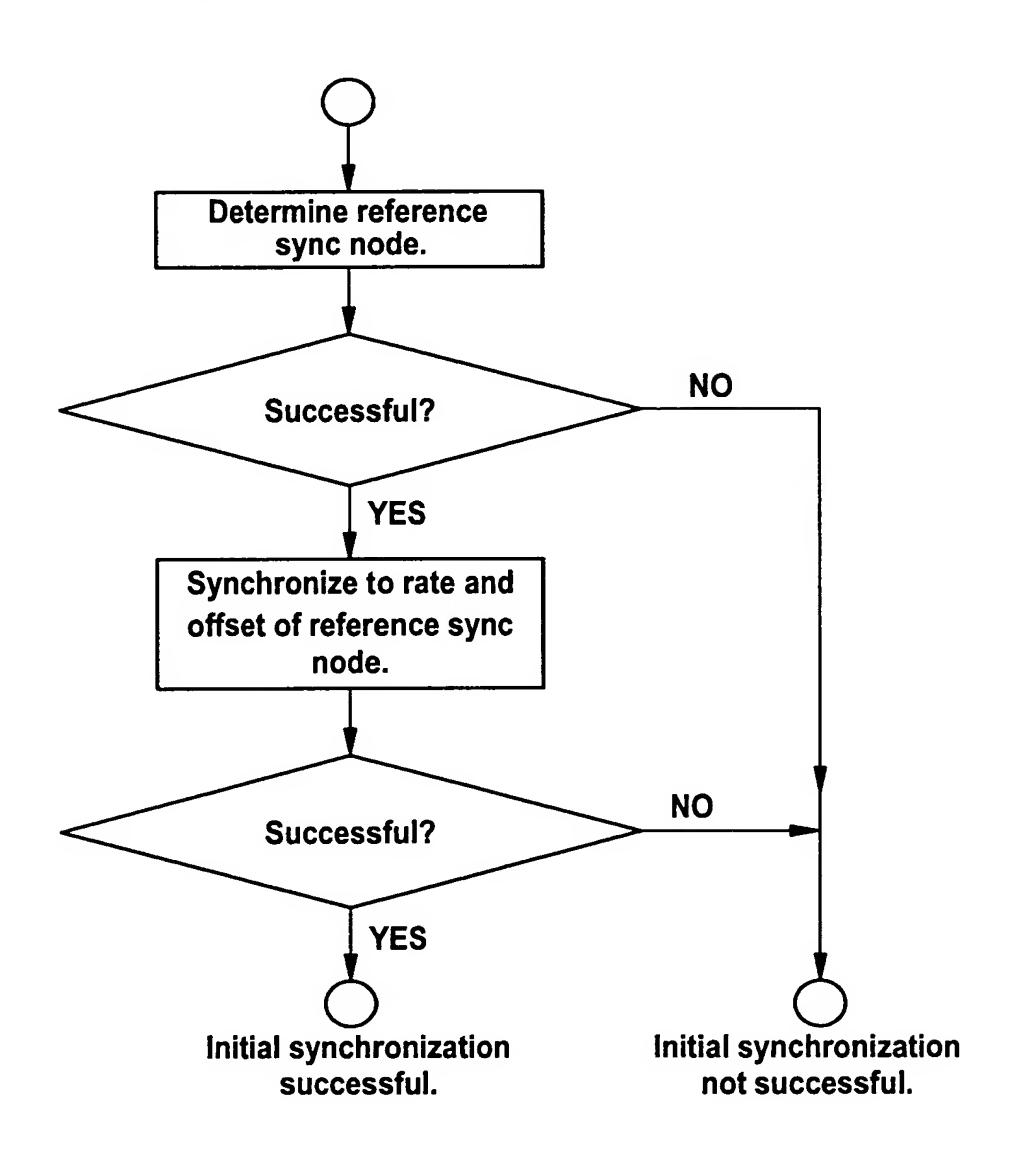


Fig. 55

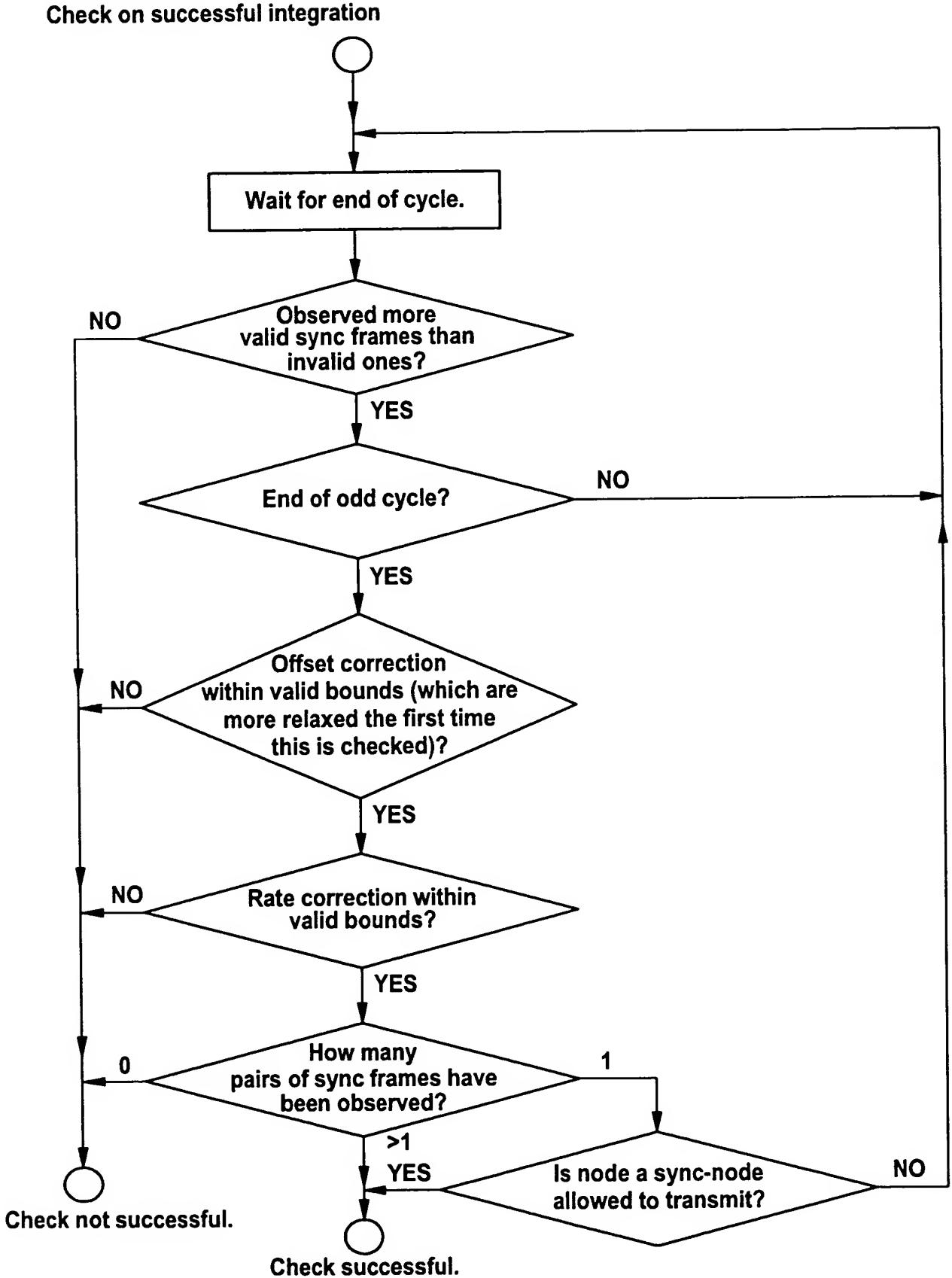
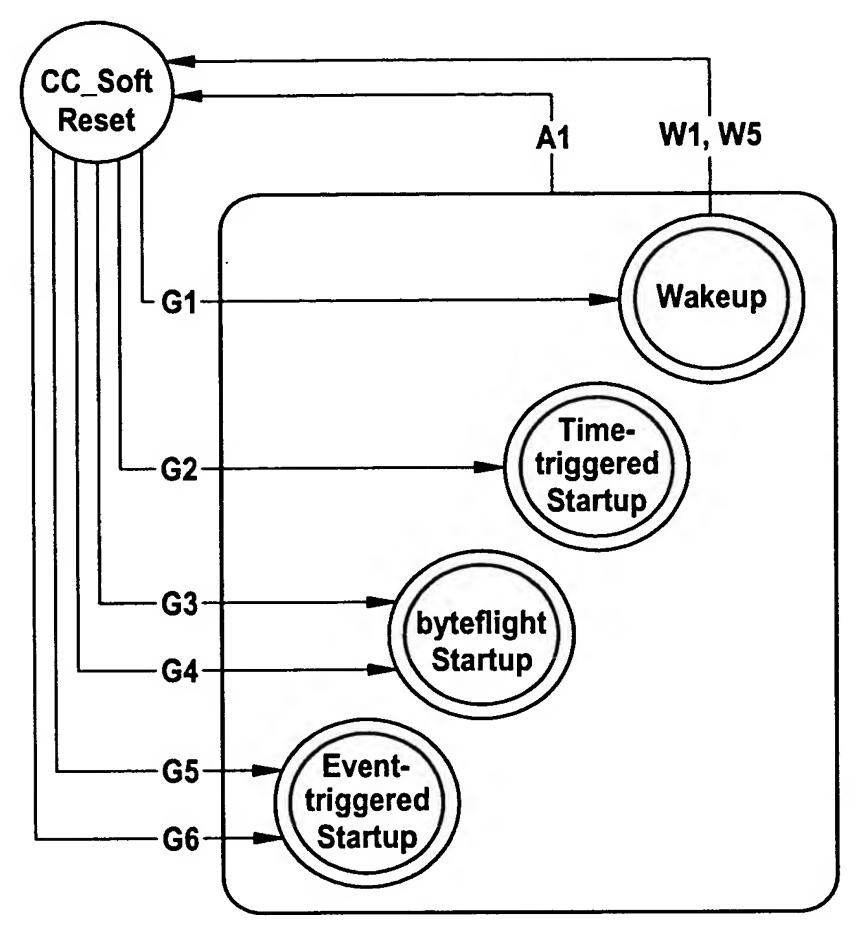


Fig. 56



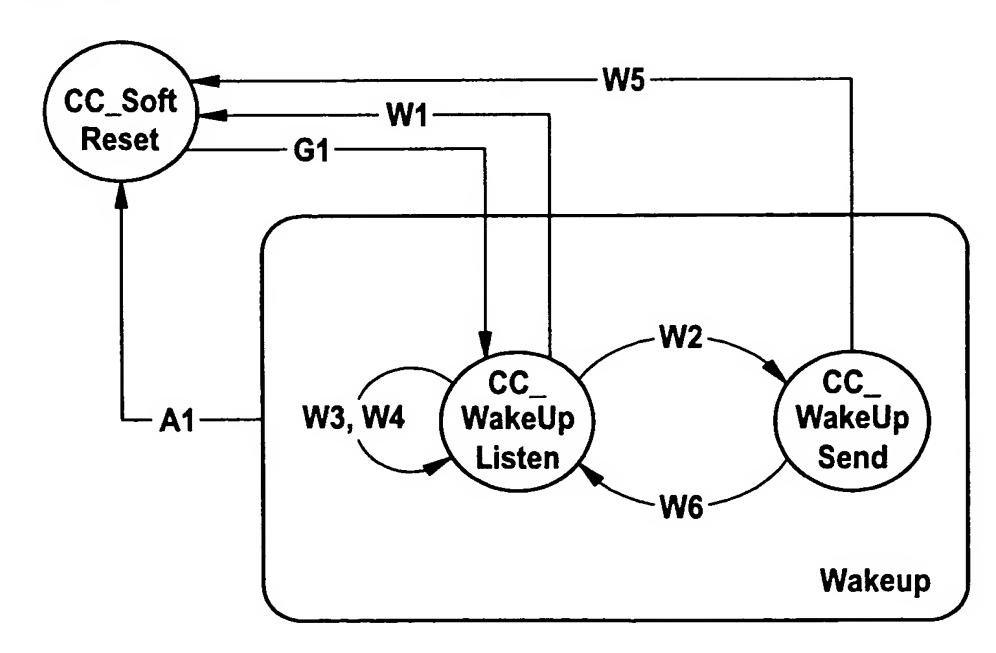
Wakeup state machine for the wakeup (WU) protocol mode

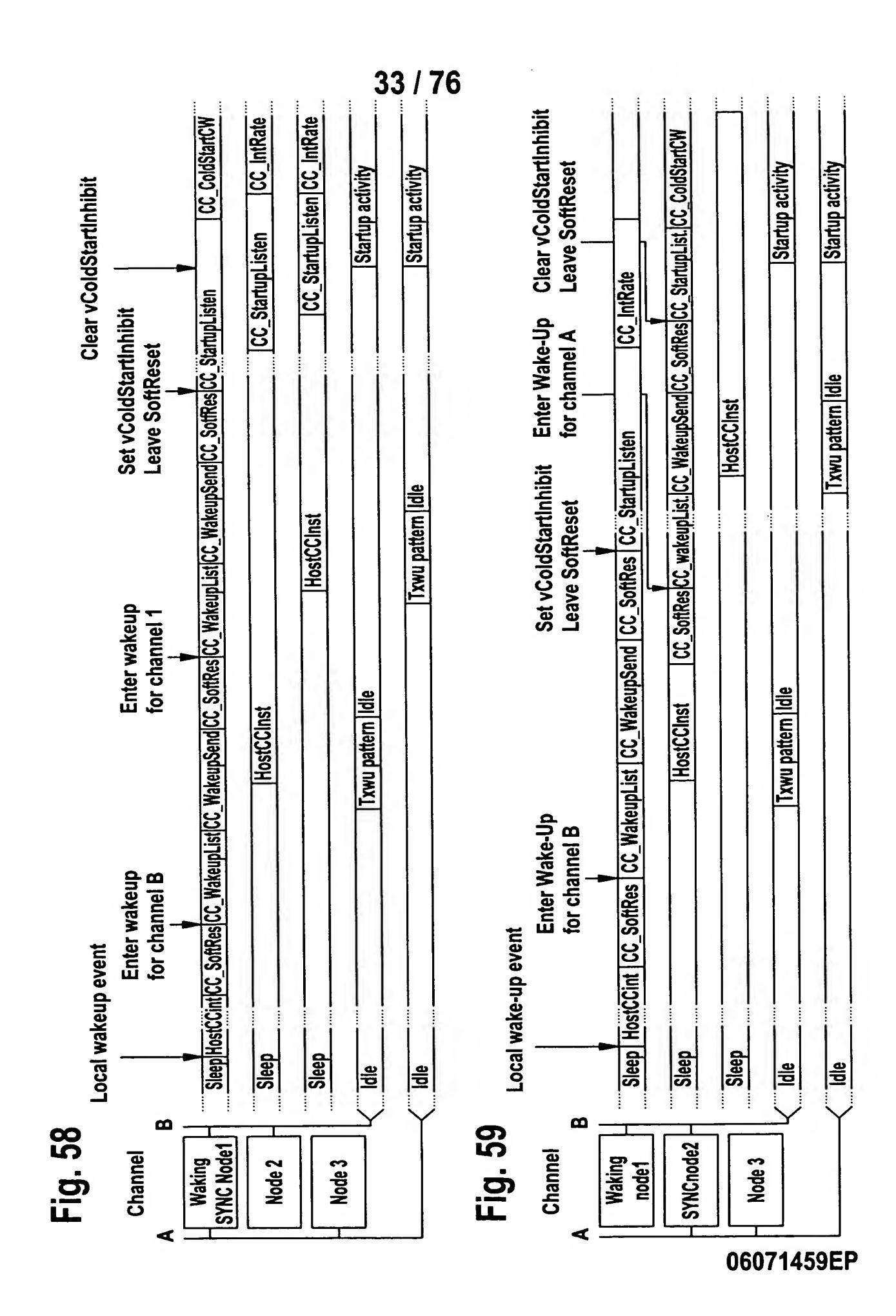
Startup state machine for the time-triggered (TT-D, TT-M) protocol modes

Startup state machine for the byteflight (BF) protocol mode

Startup state machine for the event-triggered (ET) protocol mode

Fig. 57





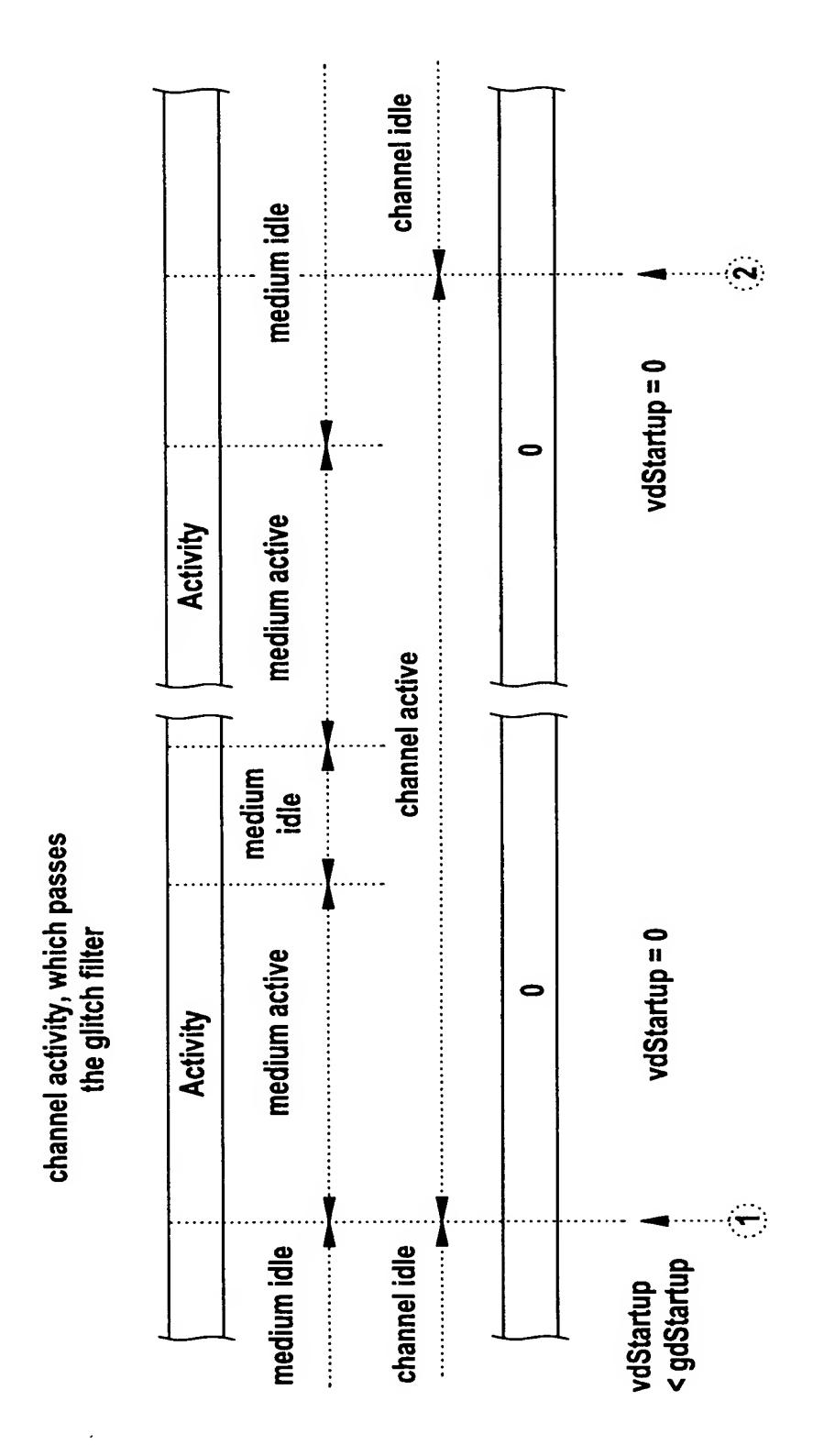


Fig. 60

06071459EP

Fig. 61

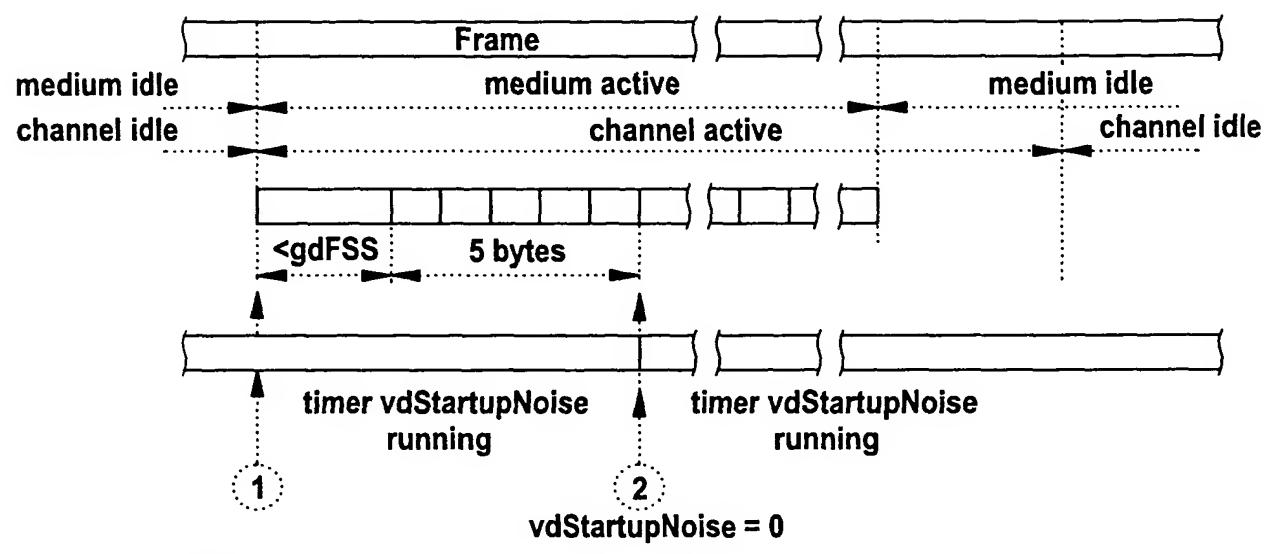


Fig. 62

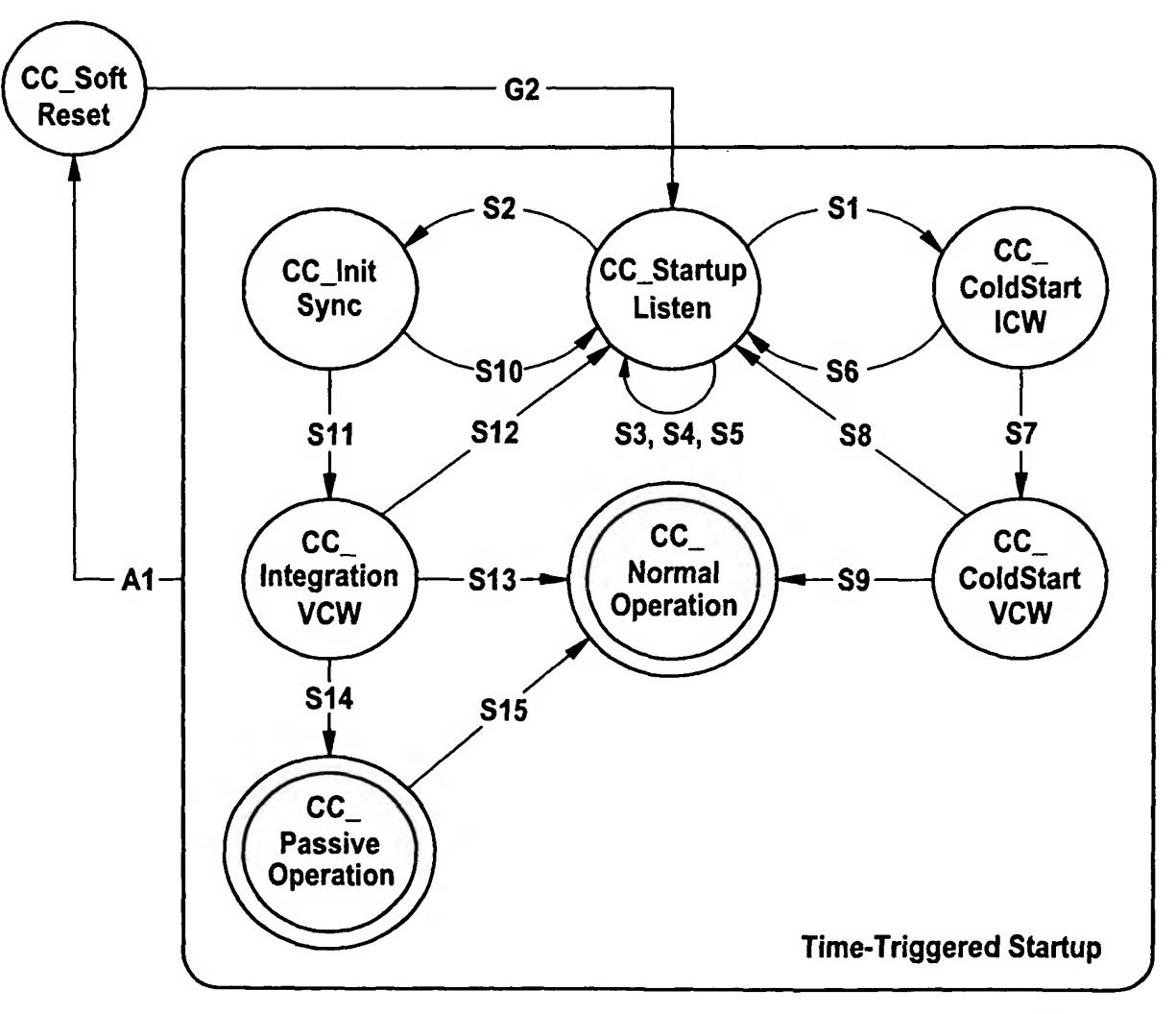


Fig. 63

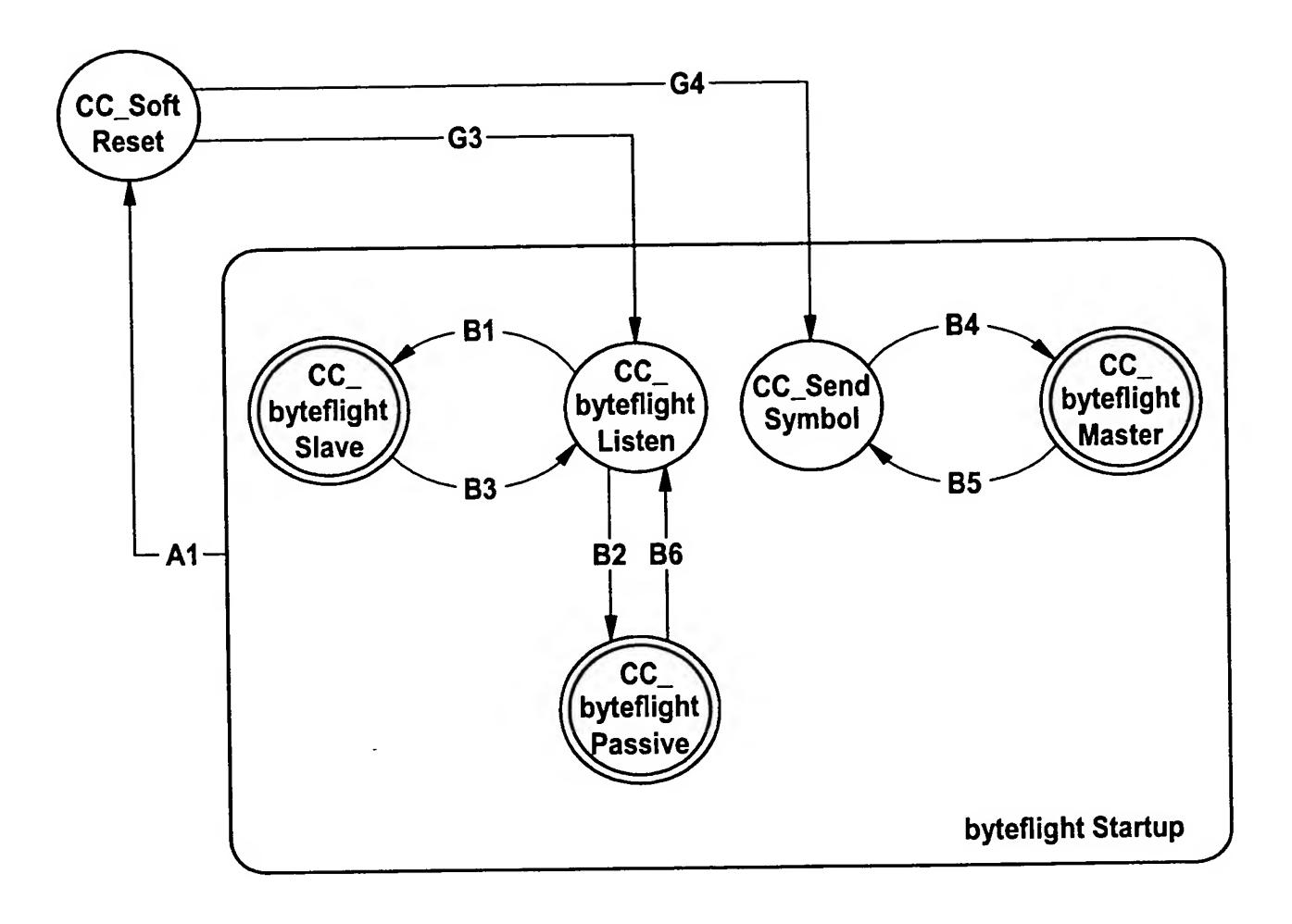
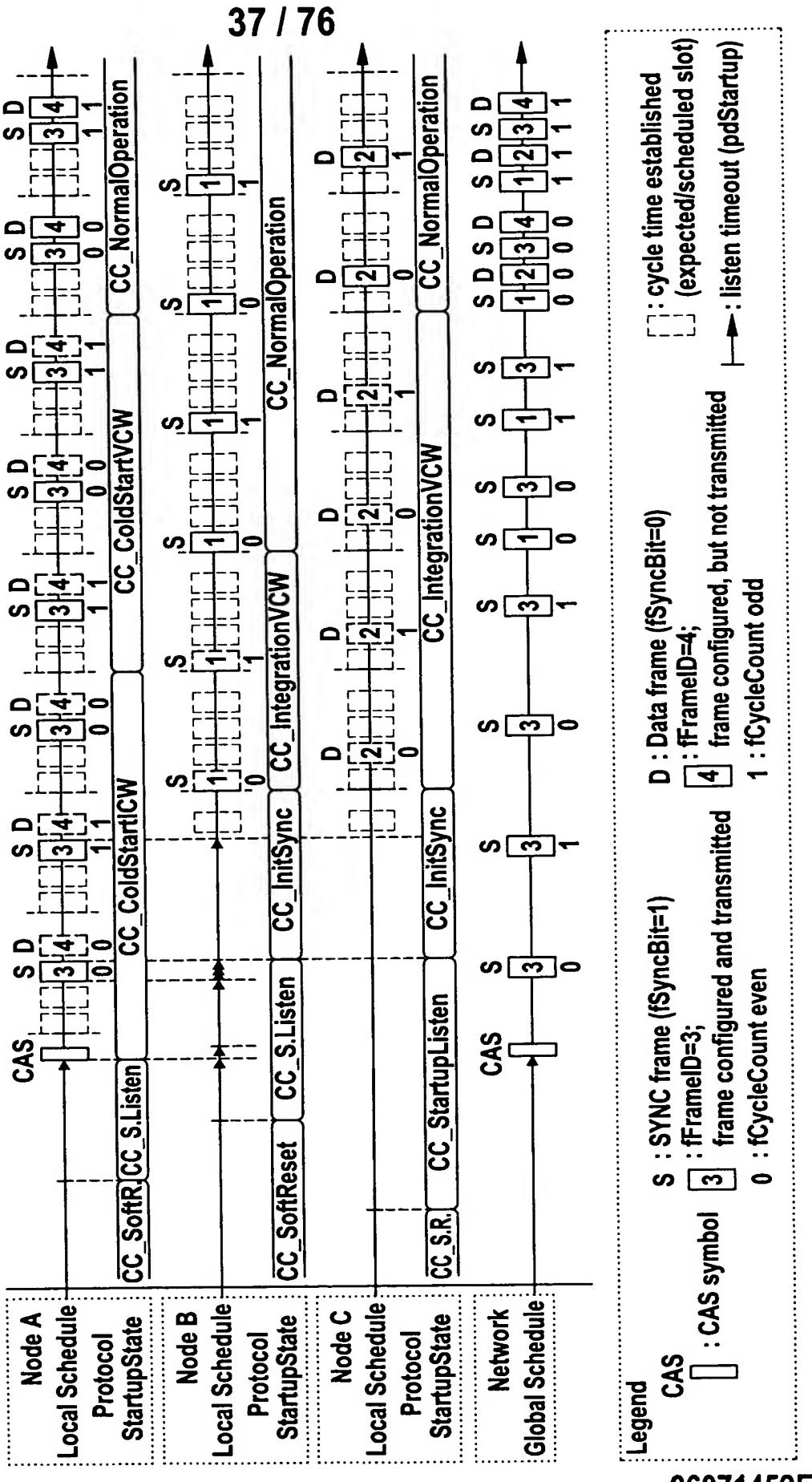


Fig. 64



06071459EP

CC_NormalOperation Normal Operation CC_NormalOperation CC_IntegrationVCW IntegrationVCW S 2 4 S 1000 IntegrationVCW CC_InitSync S လ[ညီ]ဝ S CC_StartupListen CC_Integration InitSync ဟ S 0 Coll. 0 CC_SoftR.CC_S.Listen CC_ CC S.Listen CAS CAS CC_SoftR]CC_S.Listen CC SoftReset Global Schedule **Local Schedule** Local Schedule **Local Schedule** Node C Node A Node B Network **StartupState StartupState StartupState Protocol Protocol Protocol Legend**

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Fig. 65

[]: cycle time established [] (expected/scheduled slot)

: listen timeout (pdStartup)

frame configured, but not transmitted

frame configured and transmitted

: fCycleCount even

: SYNC frame (fSyncBit=1)

S

fFrameID=3;

က

: CAS symbol

fCycleCount odd

: Data frame (fSyncBit=0)

: fFrameID=4

CC_IntegrationVCW CC IntegrationVCW യ<u>െ</u> ≁ S E O CC ColdStartVCW InitSync CC InitSync S E တက S E 0 တကြာလ CC StartupListen **StartupListen** SOT 0 CC Int.VCW CC_Int.VCW Failure ËE S ٥[مَ]٥ တ tic¥ InitSync CC_InitSync ColdStar S လ<u>ြဲ (</u> S CC_StartupListen CC_StartupListen CAS CAS CC SoftR CC S.Listen CC SoftReset CC_Soft. **Global Schedule** Local Schedule Local Schedule **Local Schedule** Node C Node B Node A Protocol StartupState **Network StartupState StartupState Protocol** Protocol

39 / 76

Fig. 66

[]: cycle time established [] (expected/scheduled slot)

: listen timeout (pdStartup)

frame configured, but not transmitted

frame configured and transmitte

: fCycleCount even

: SYNC frame (fSyncBit=1)

: fFrameID=3;

3

: CAS symbol

Legend

: fCycleCount odd

: Data frame (fSyncBit=0)

fFrameID=4

Fig. 67

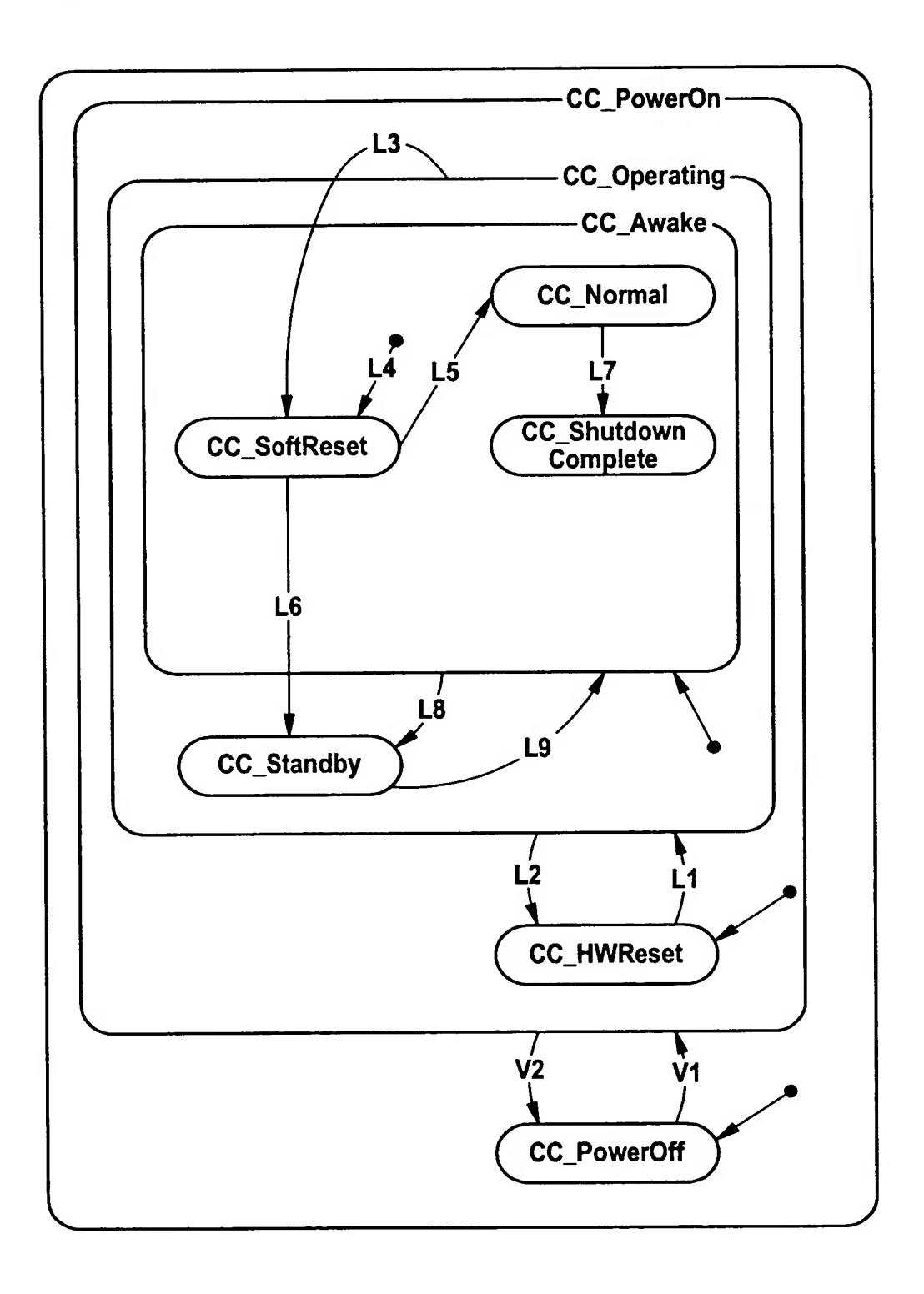


Fig. 68

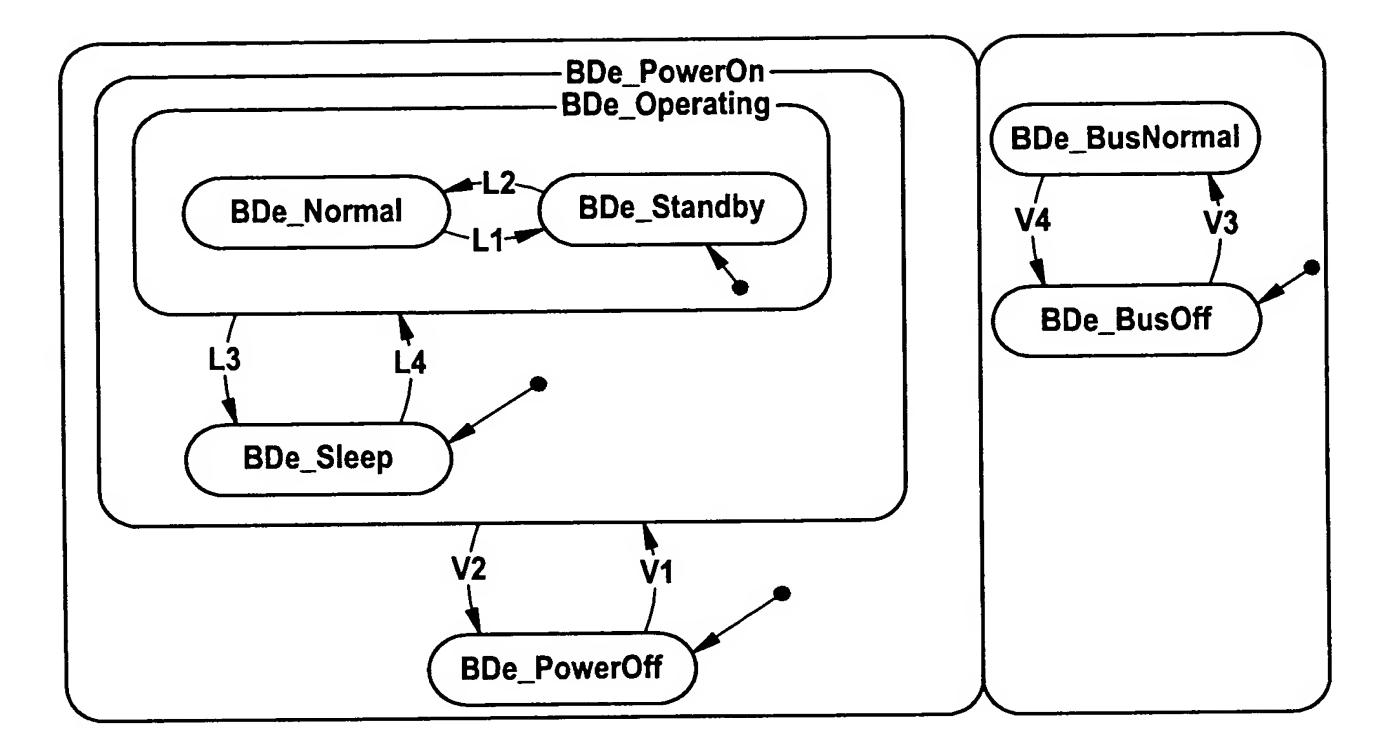


Fig. 69

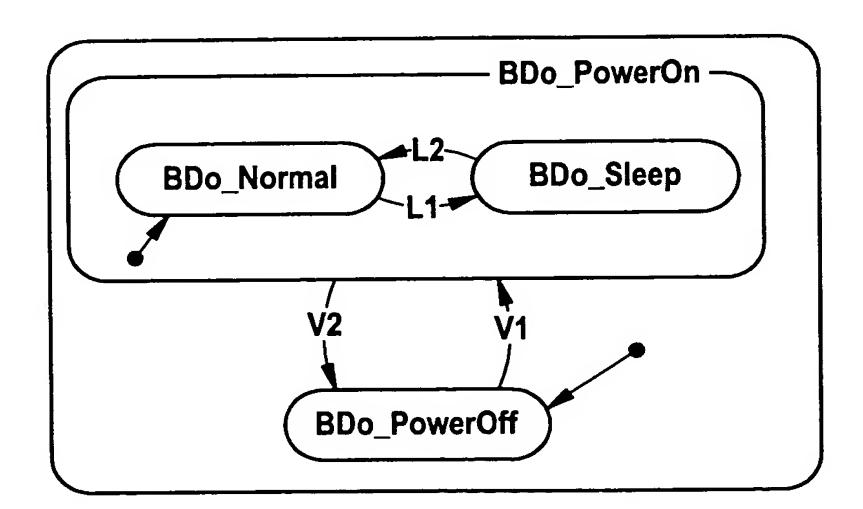


Fig. 70

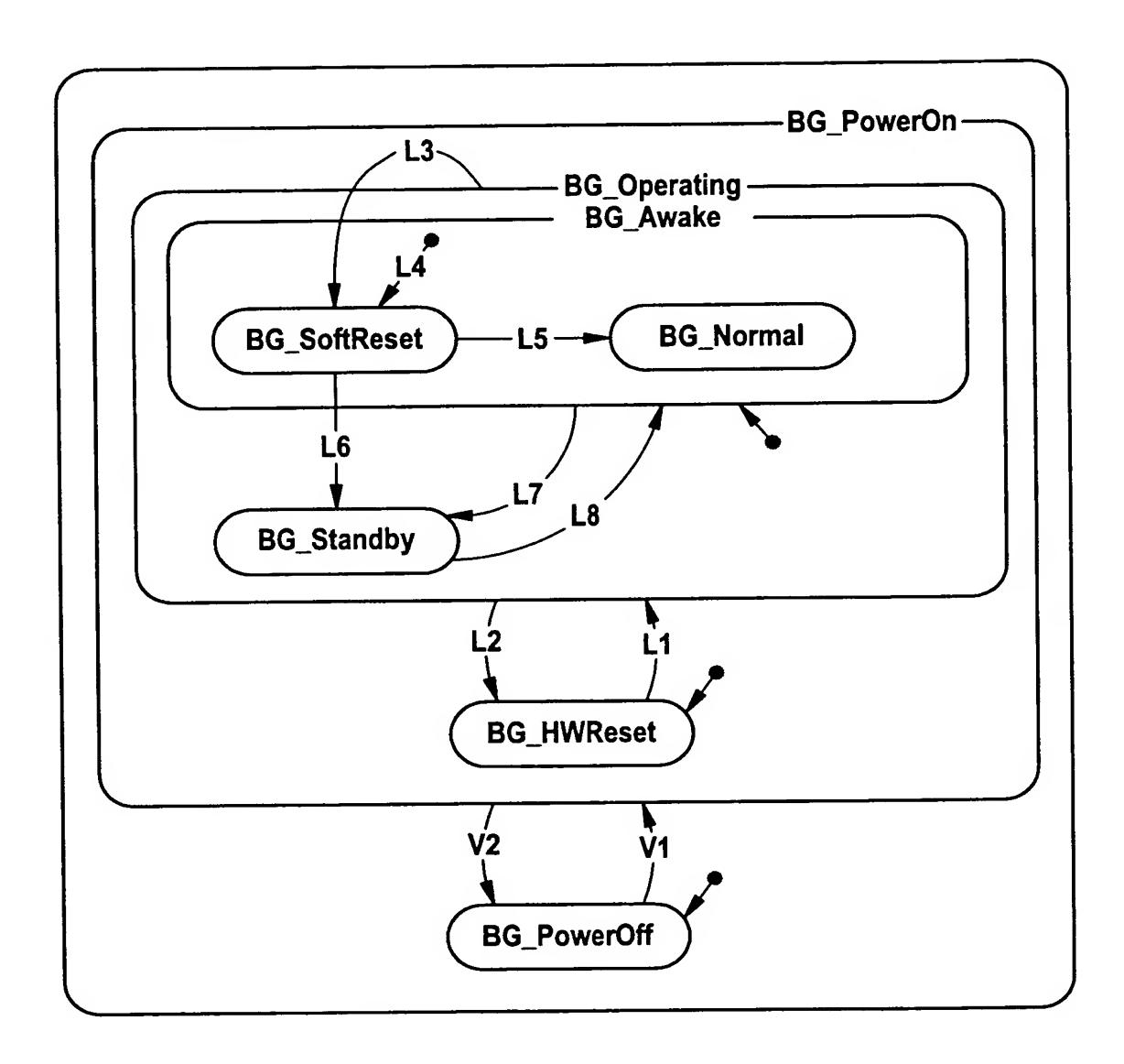


Fig. 71

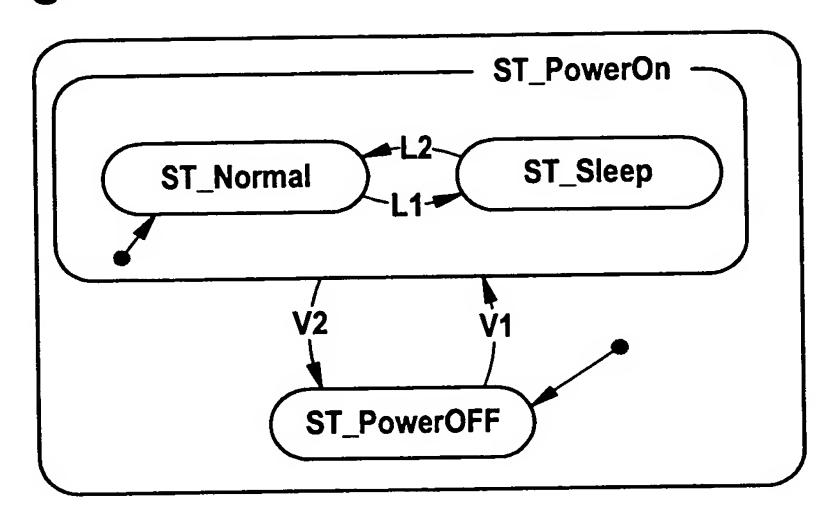


Fig. 72

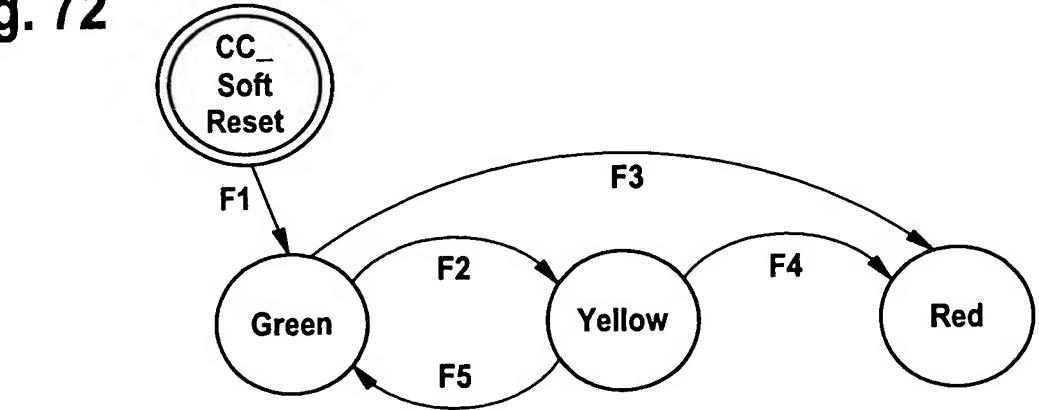
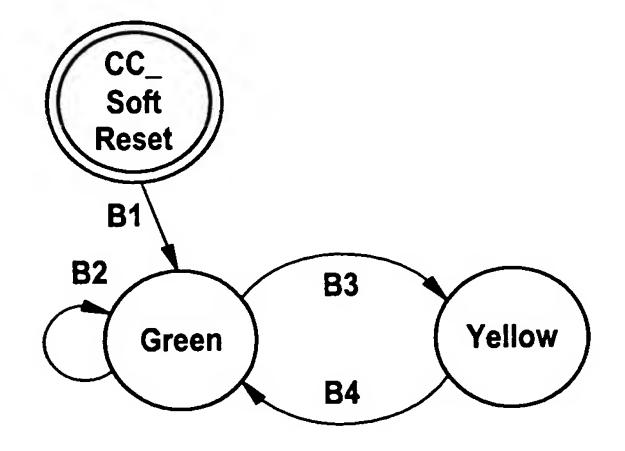


Fig. 73



Host Processor

Host Processor Interface

CHI Status Data Control Data Handling Handling Handling

Protocol Engine Interface

Protocol Engine

Fig. 75

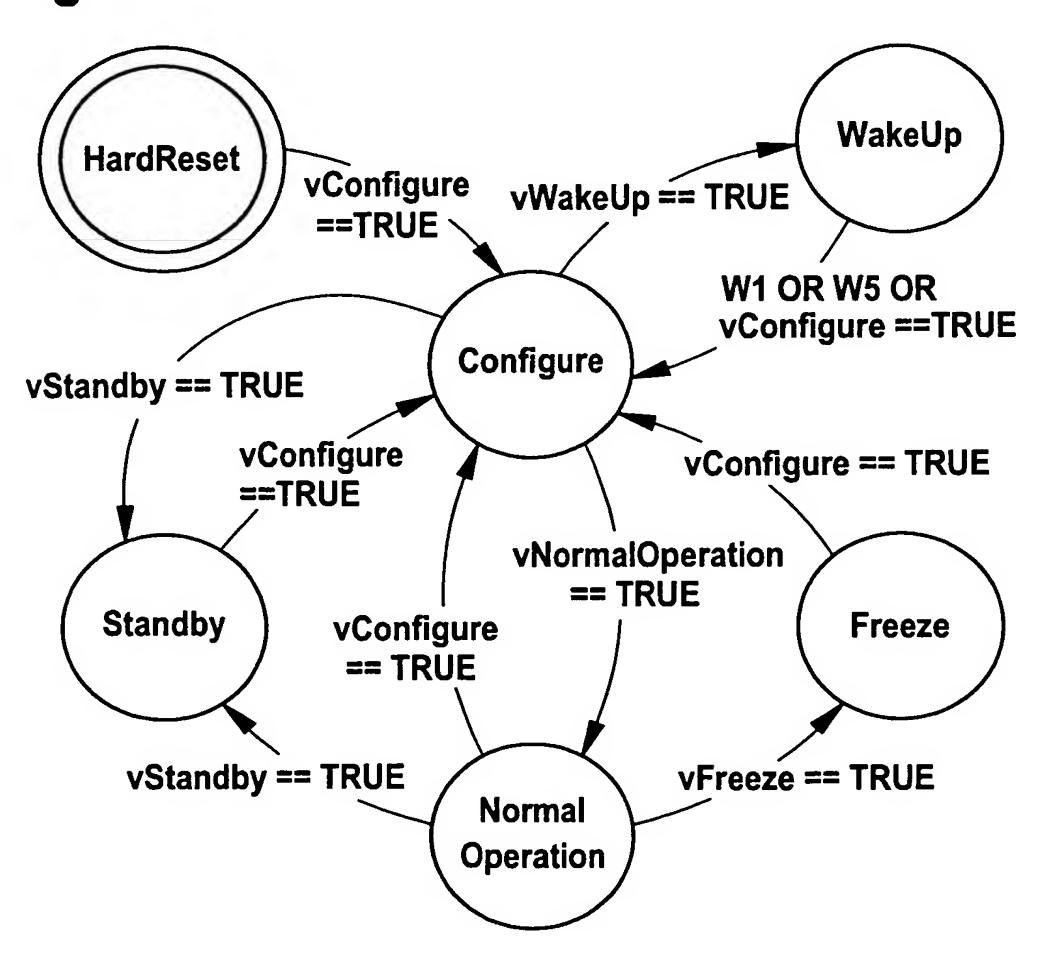


Fig. 76

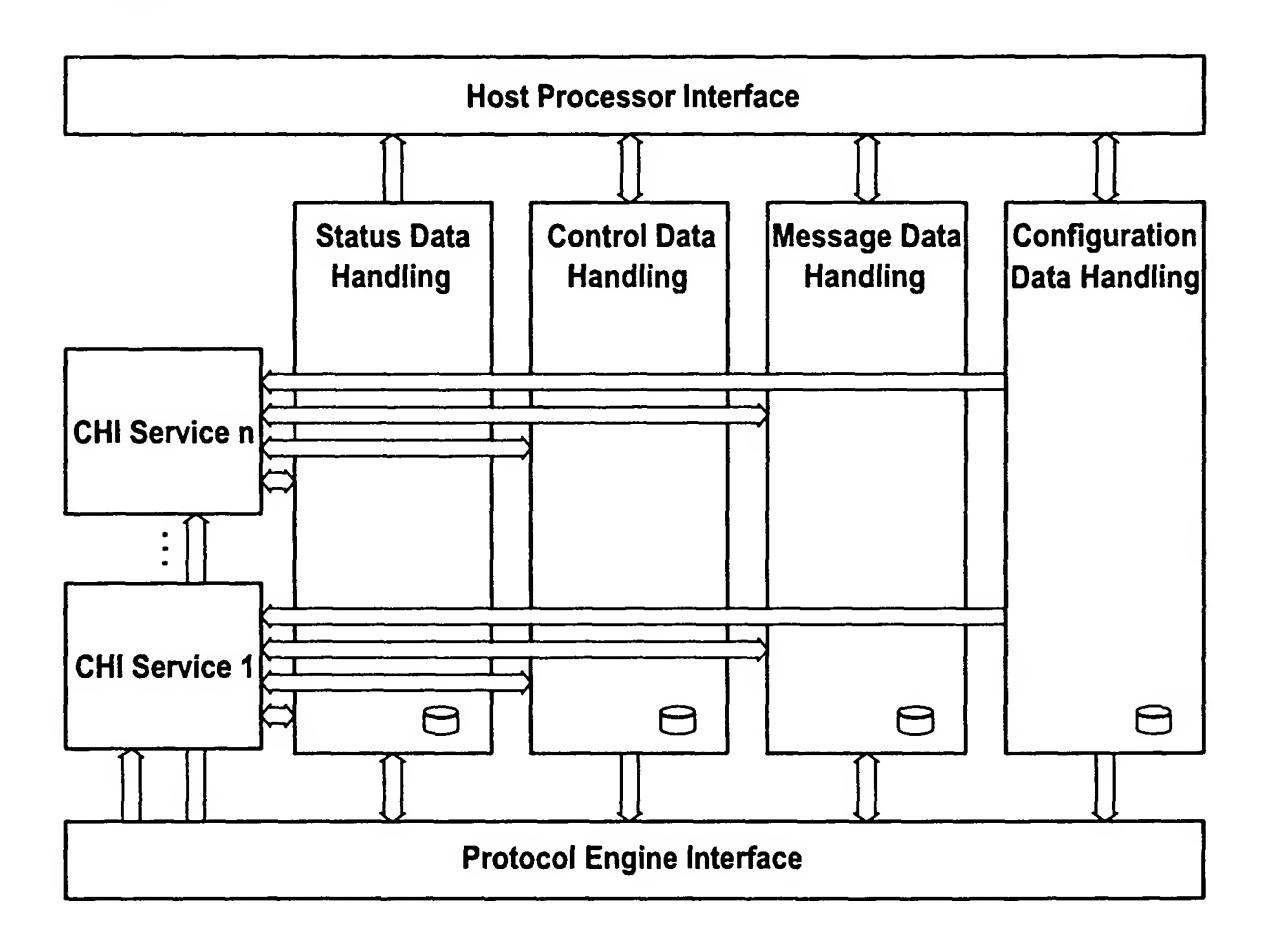


Fig. 77

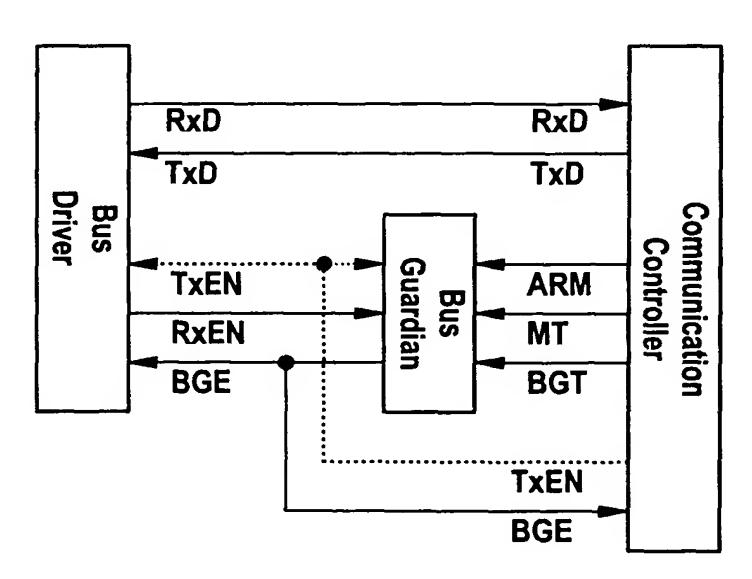


Fig. 78

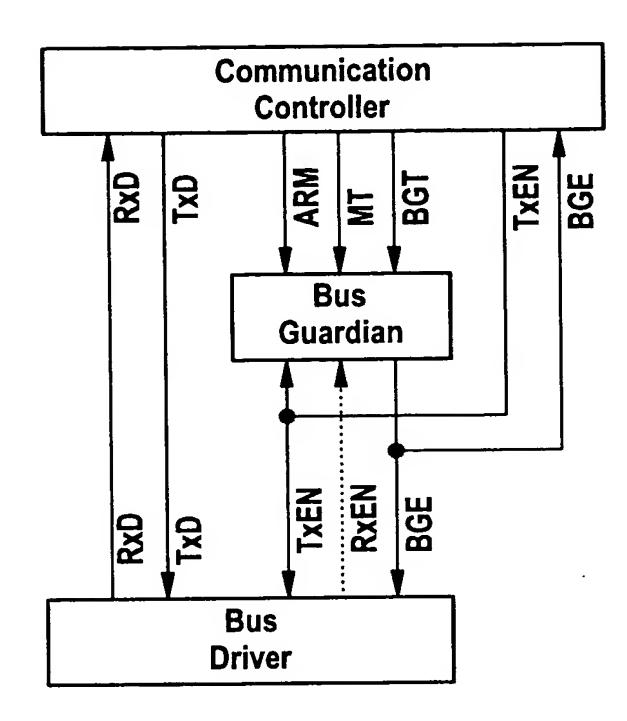


Fig. 79

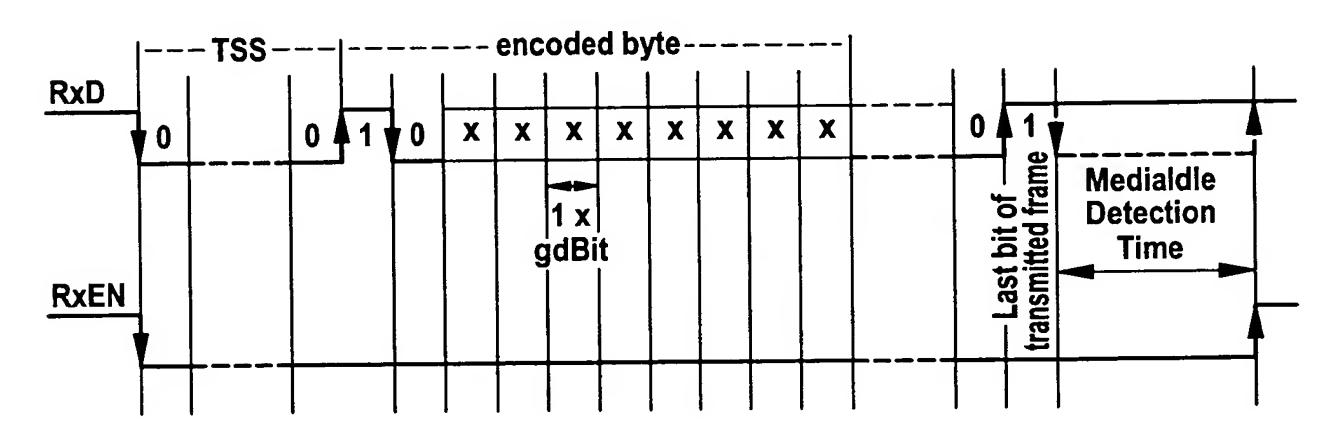


Fig. 80

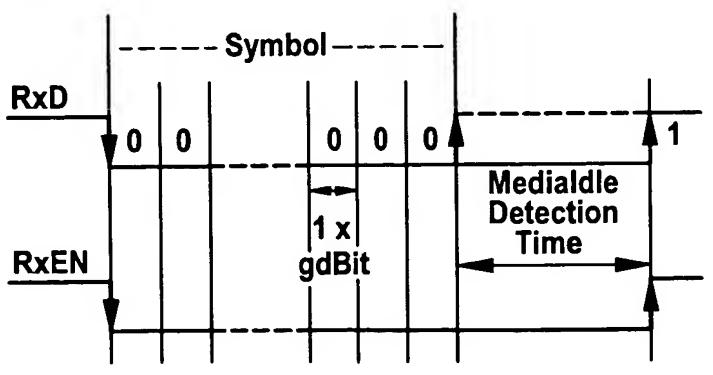


Fig. 81

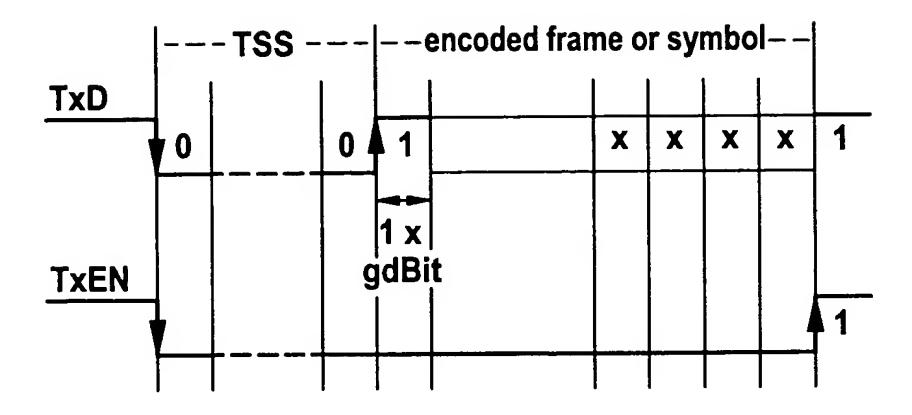
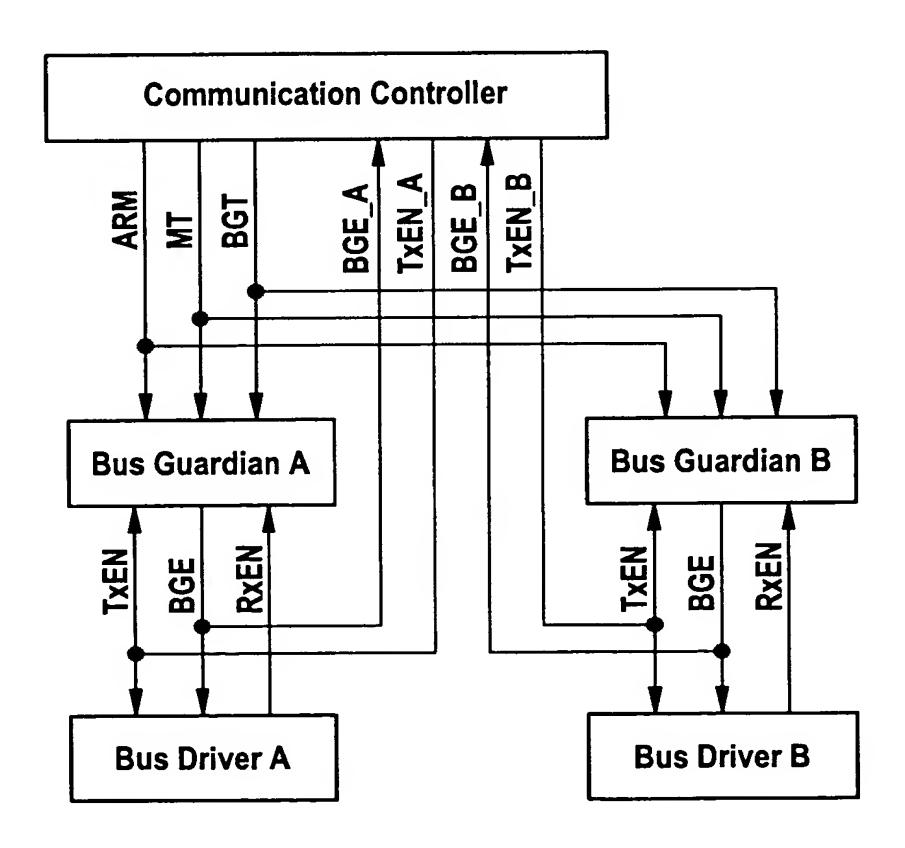
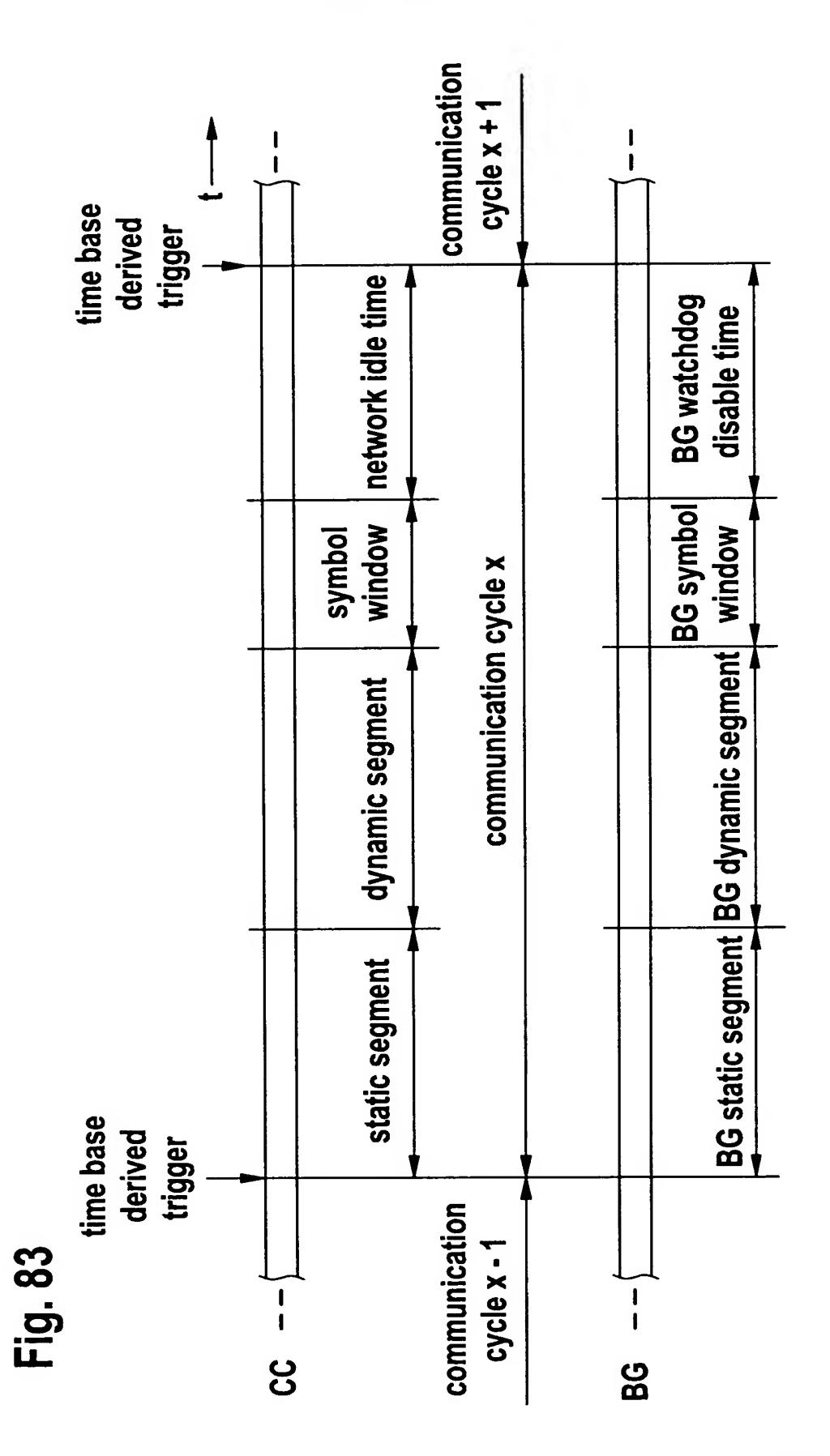
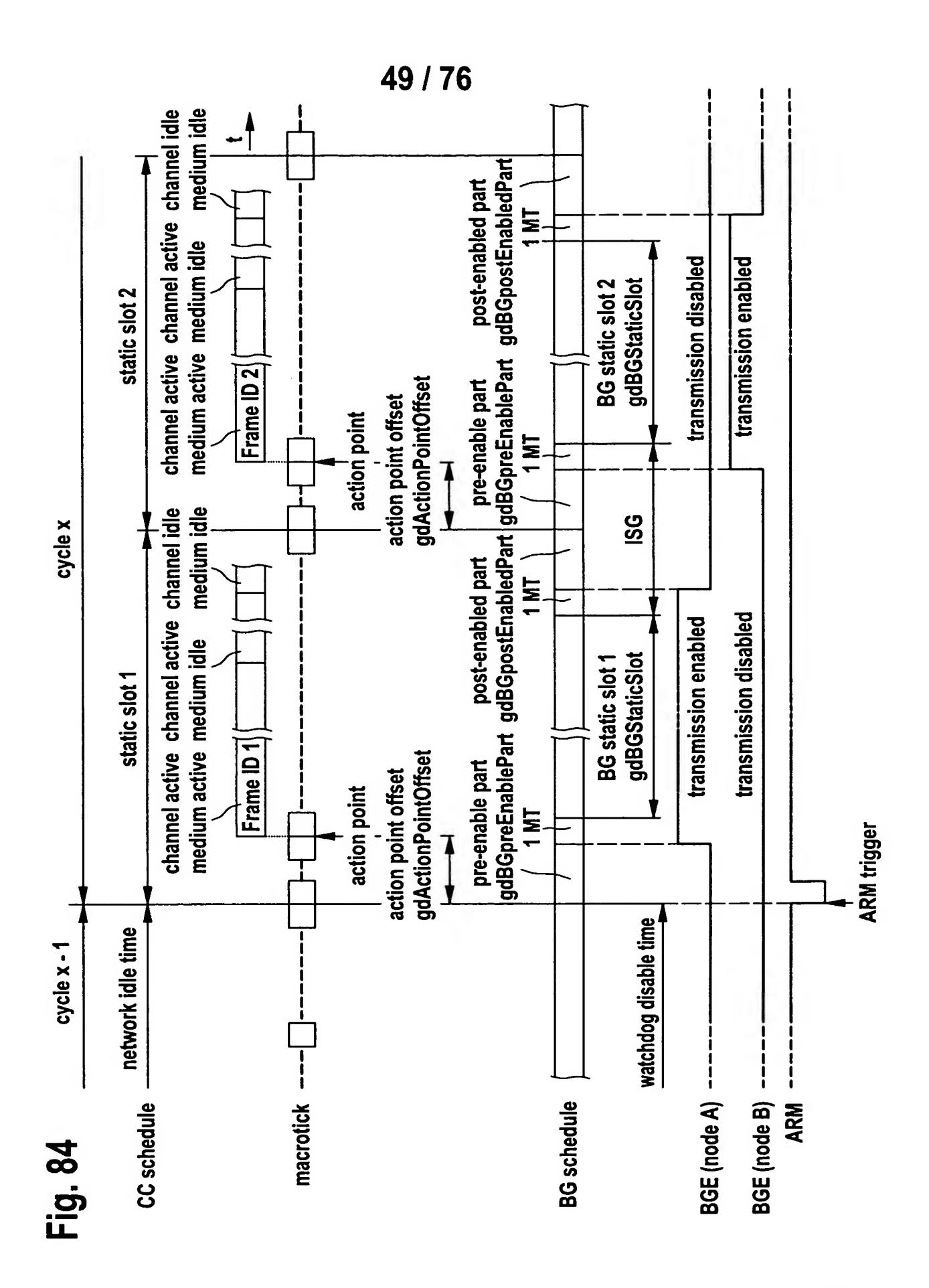
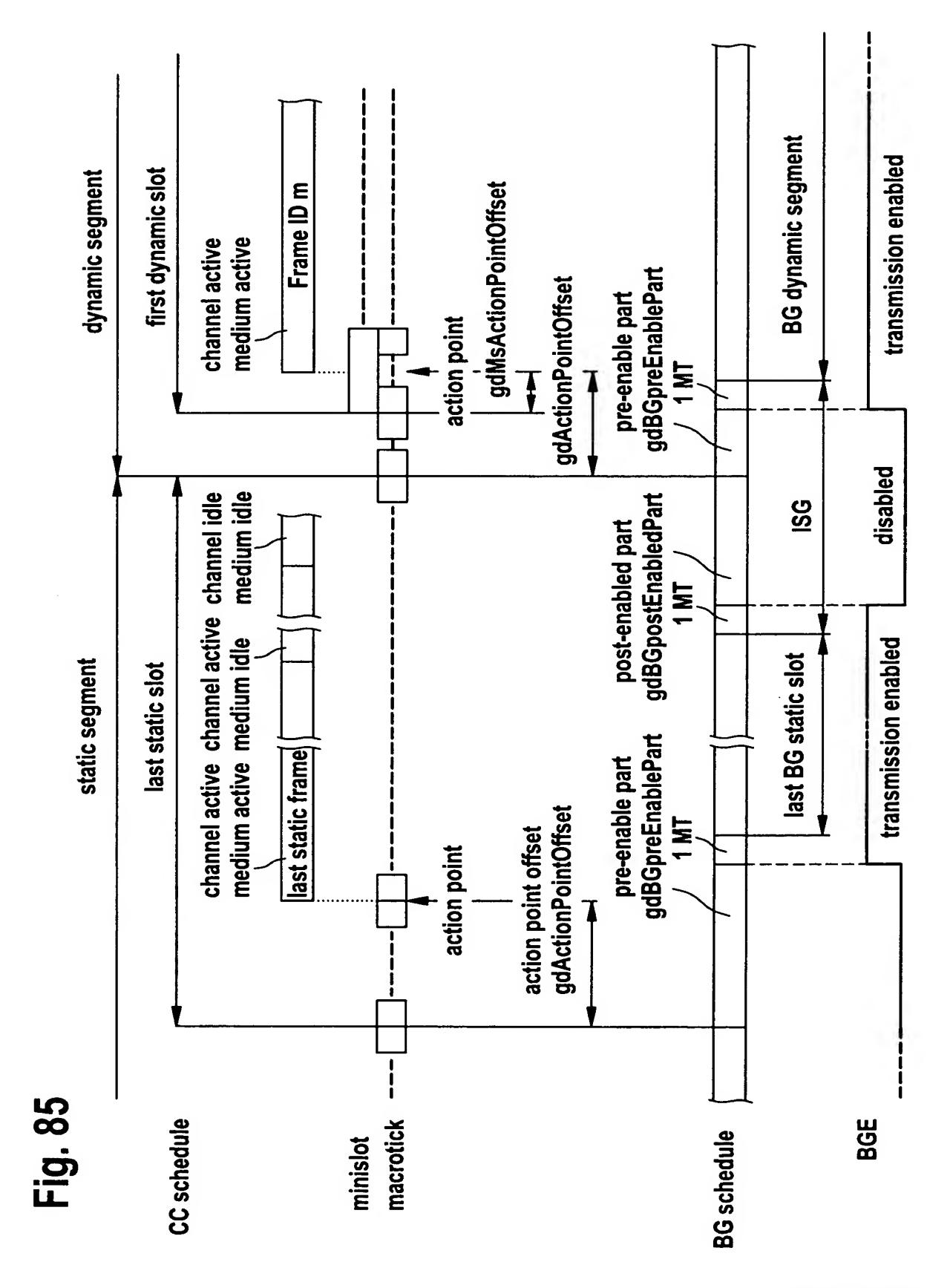


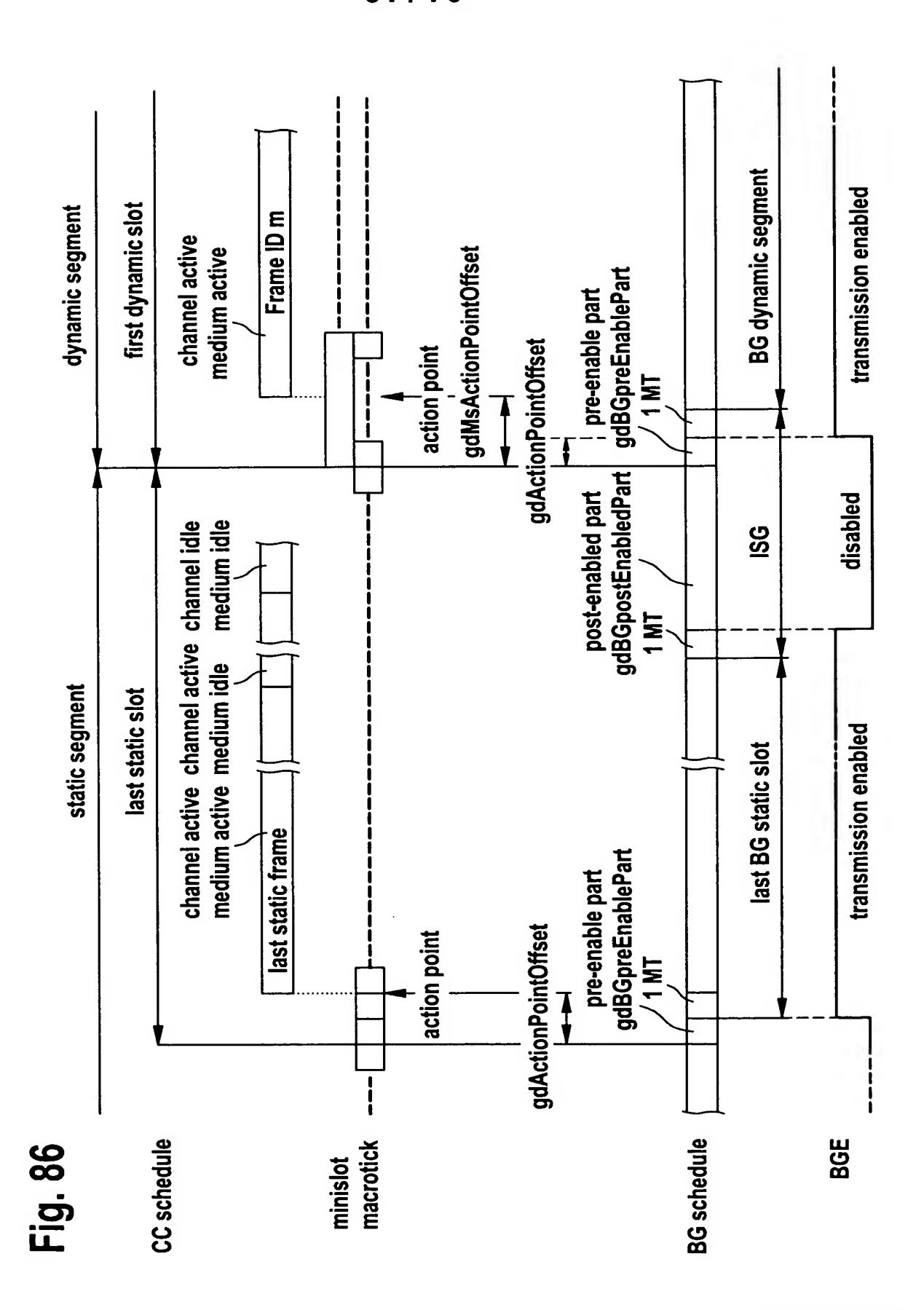
Fig. 82

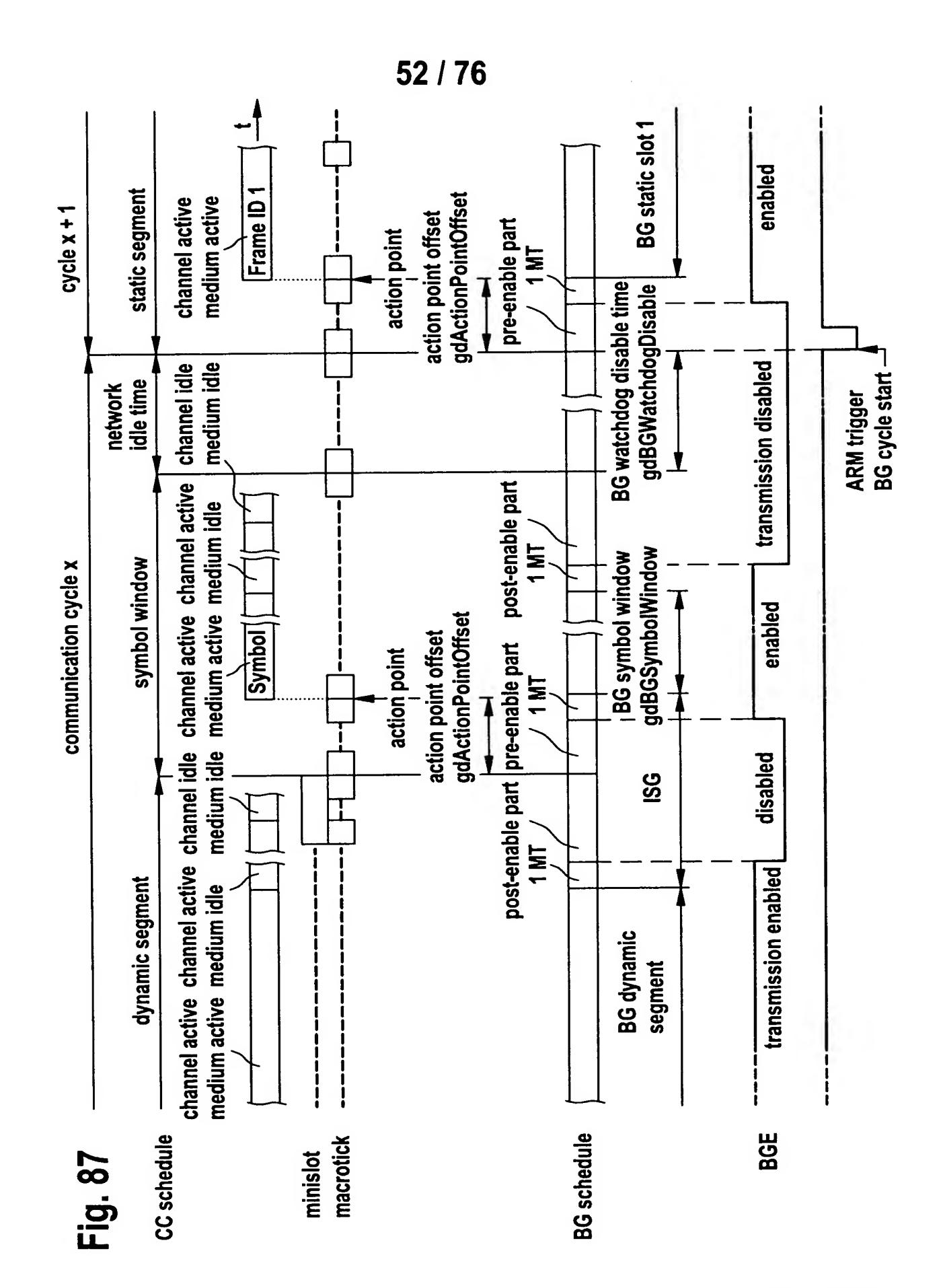












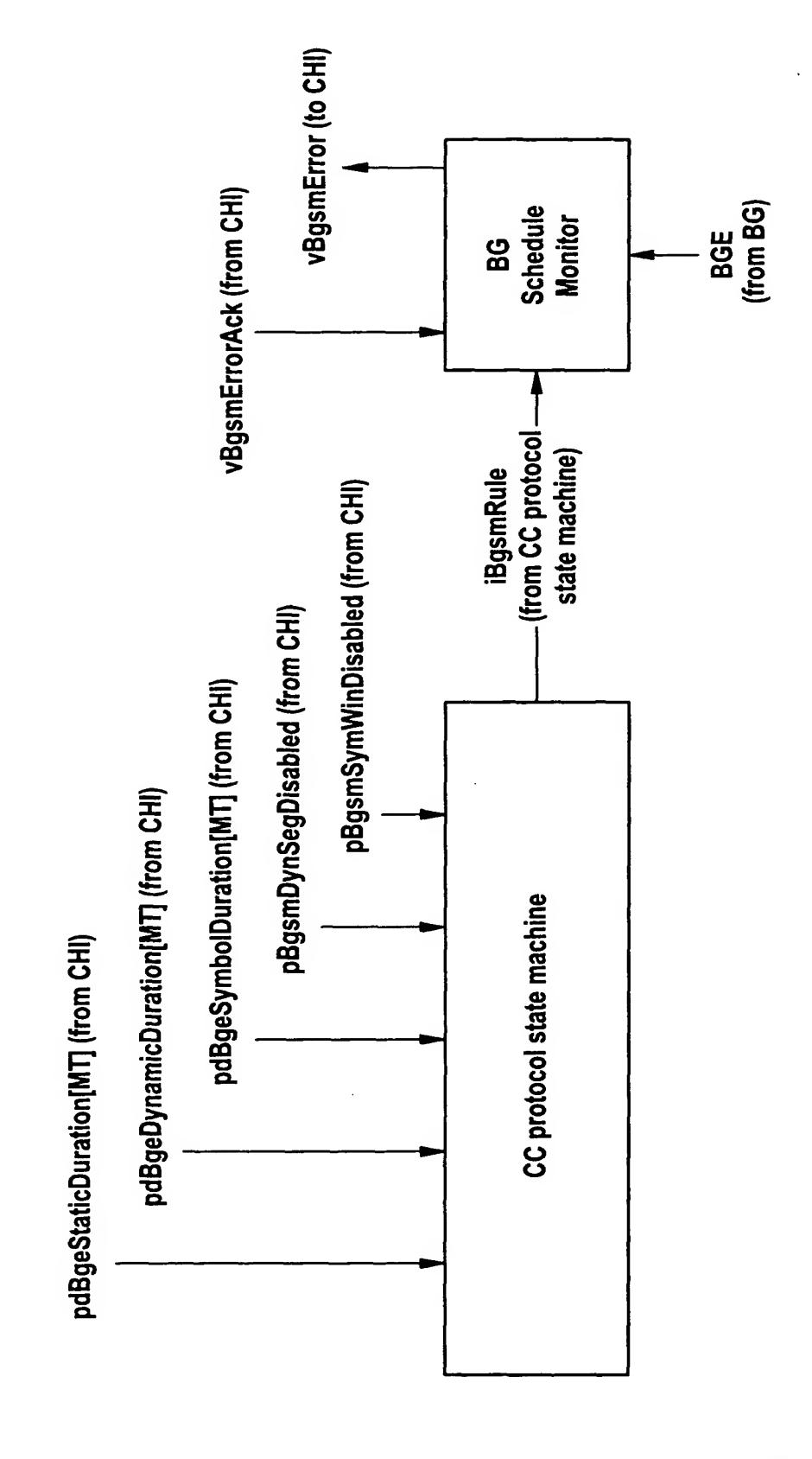


Fig. 88



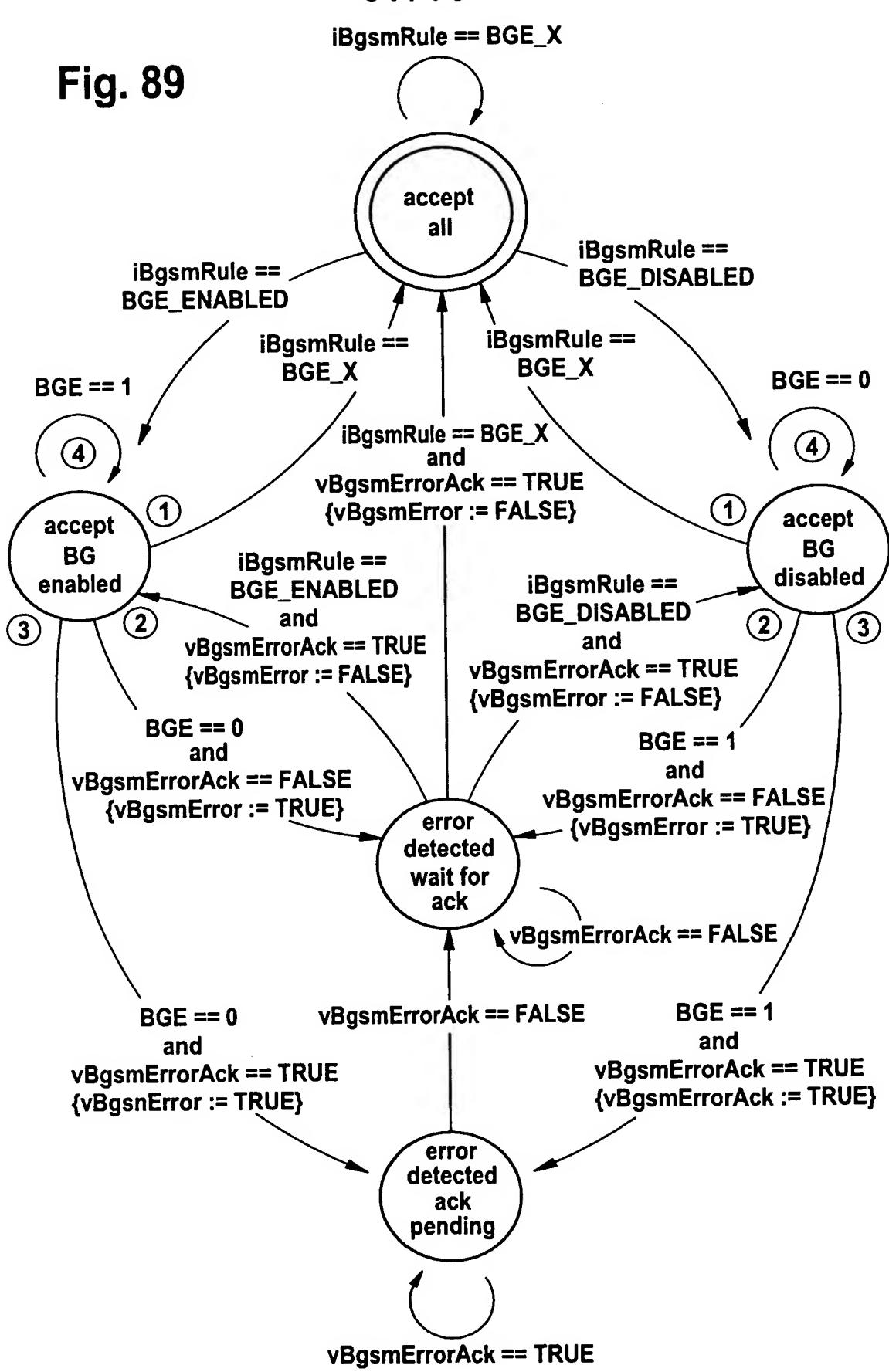
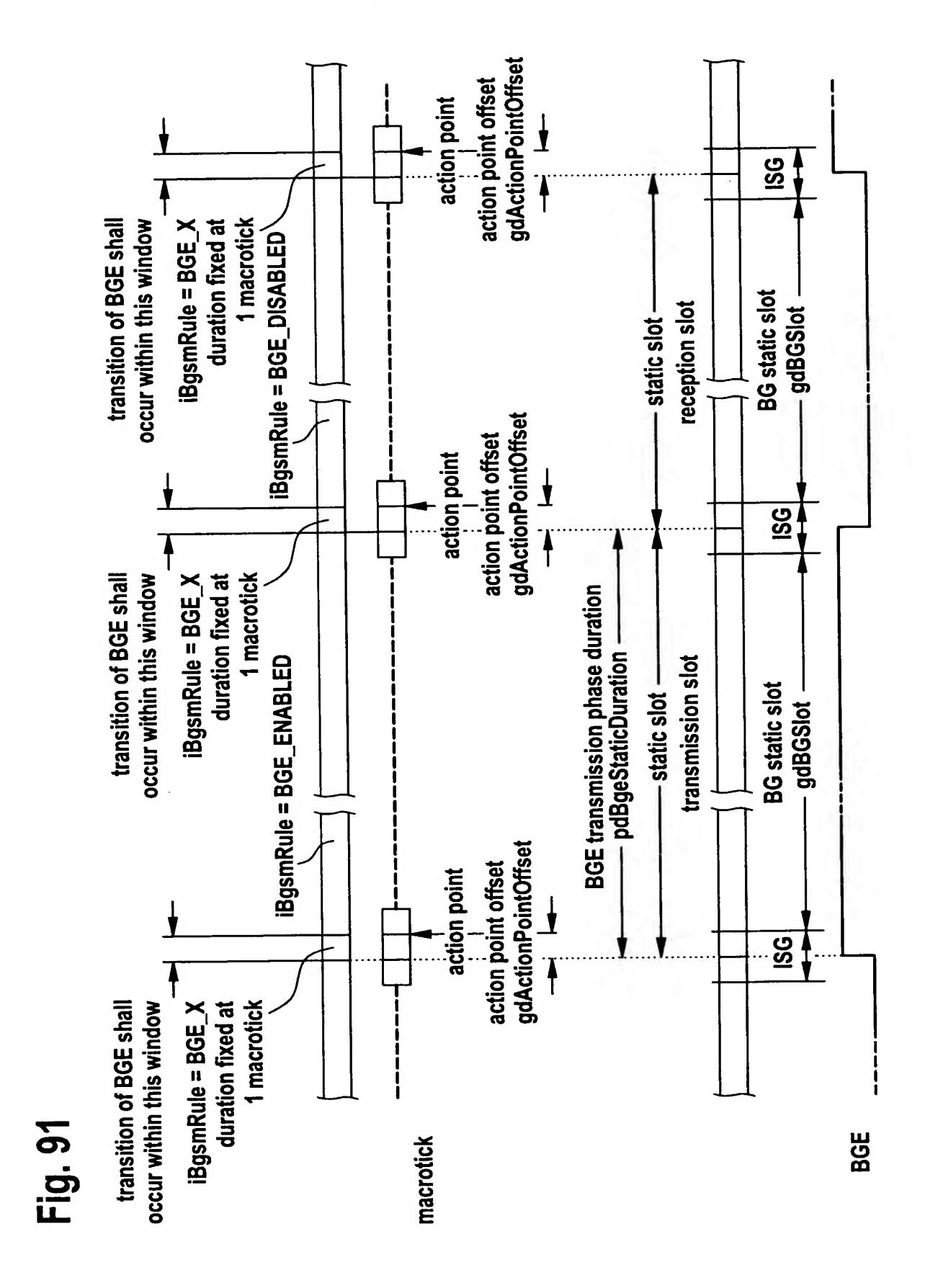
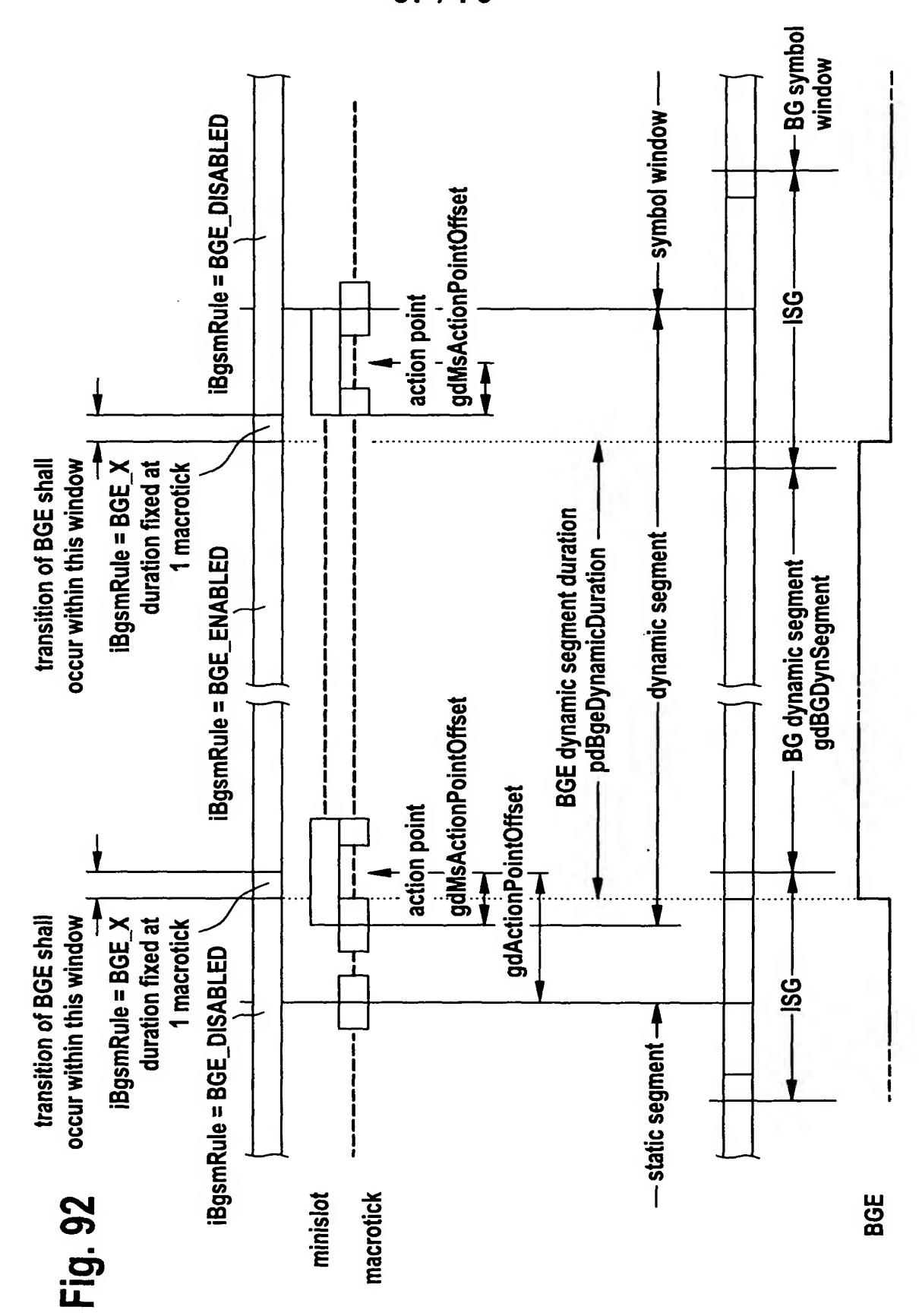


Fig. 90





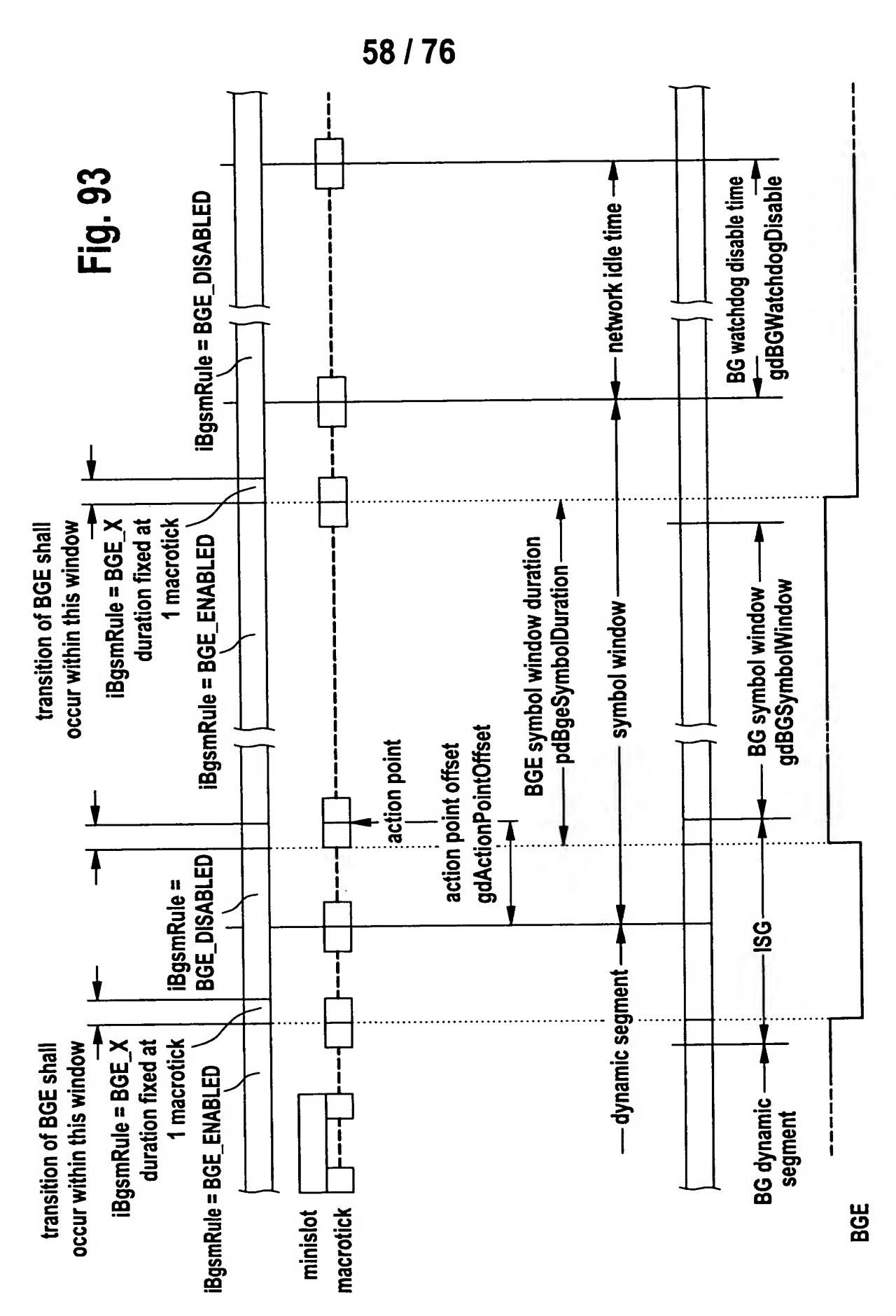


Fig. 94

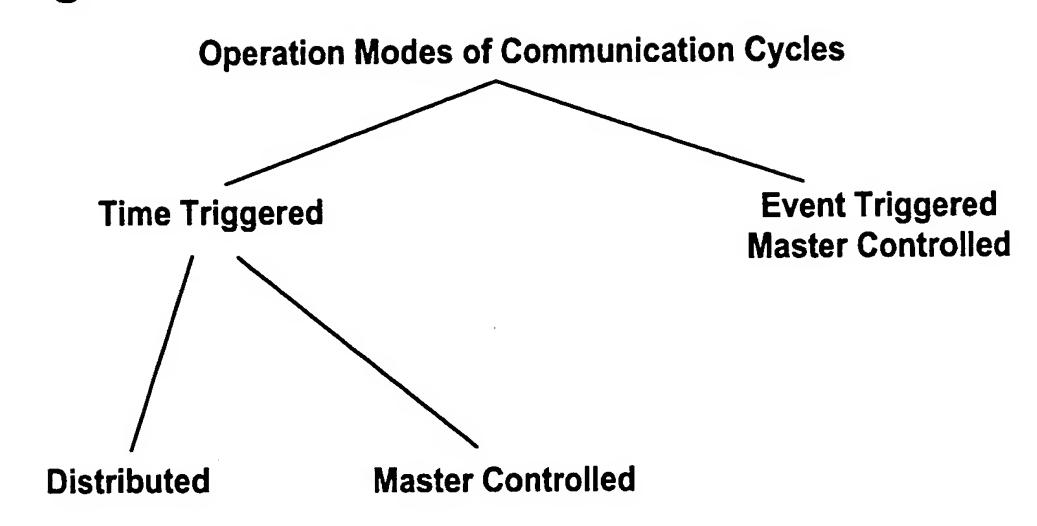
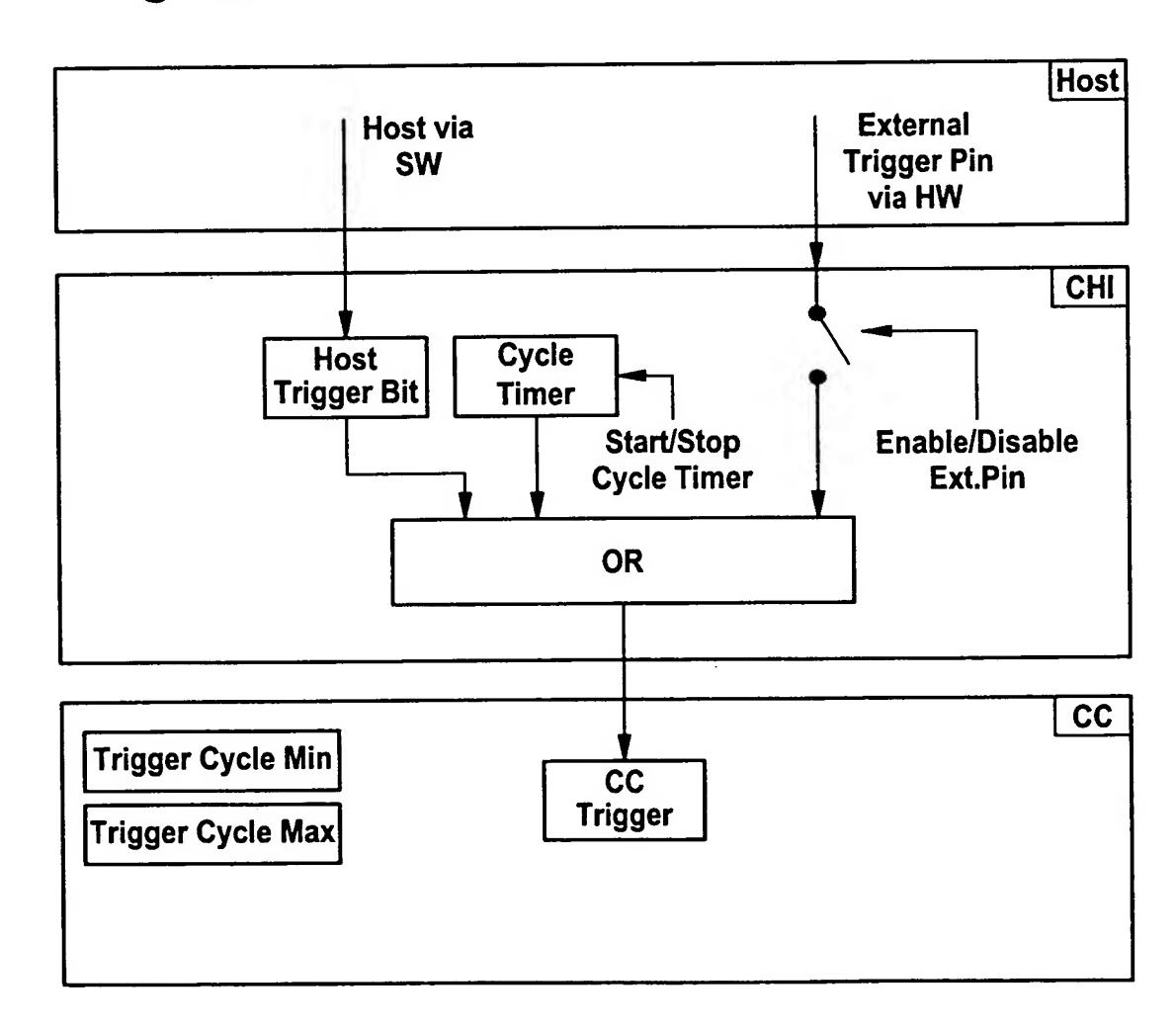
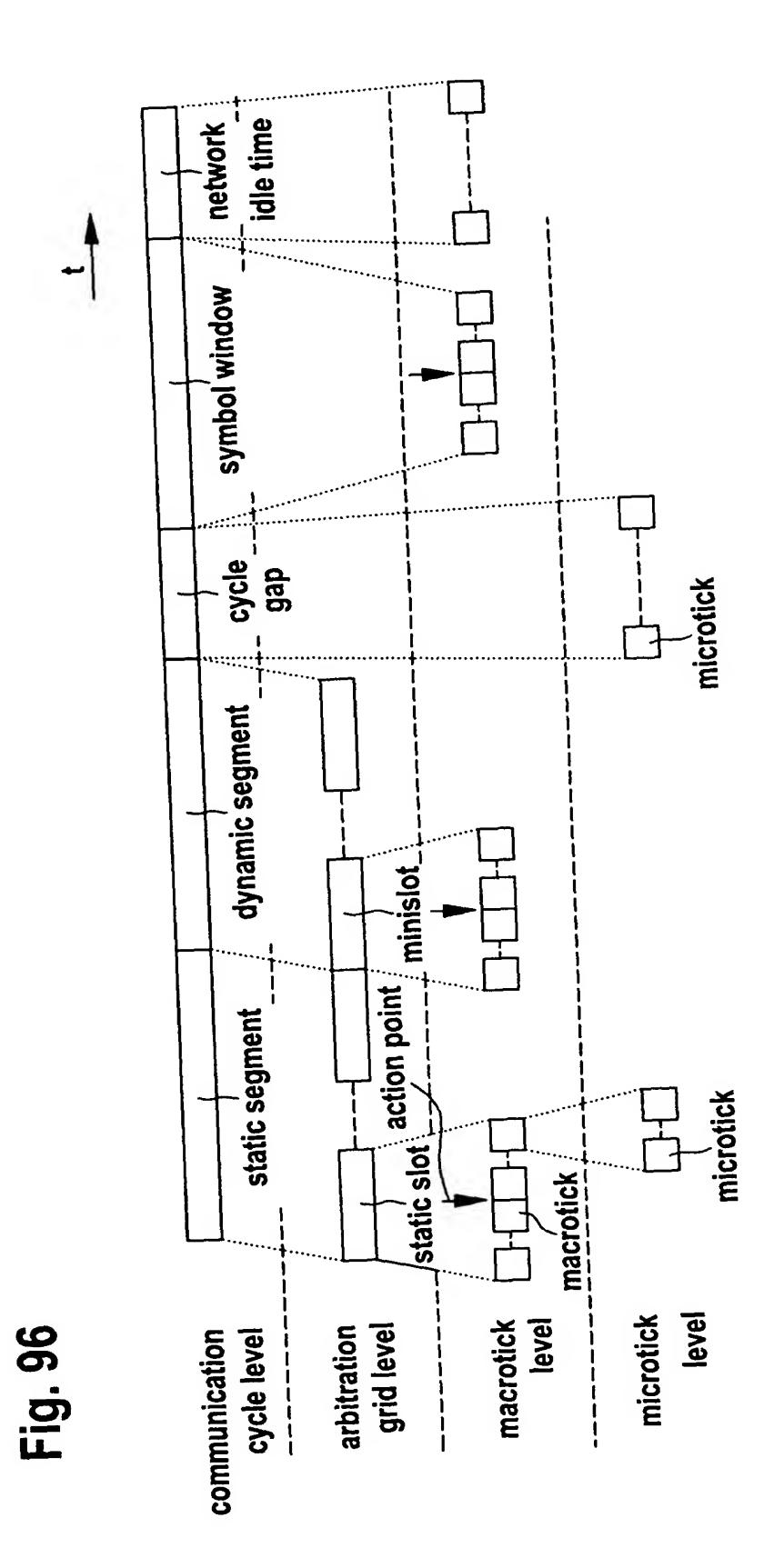
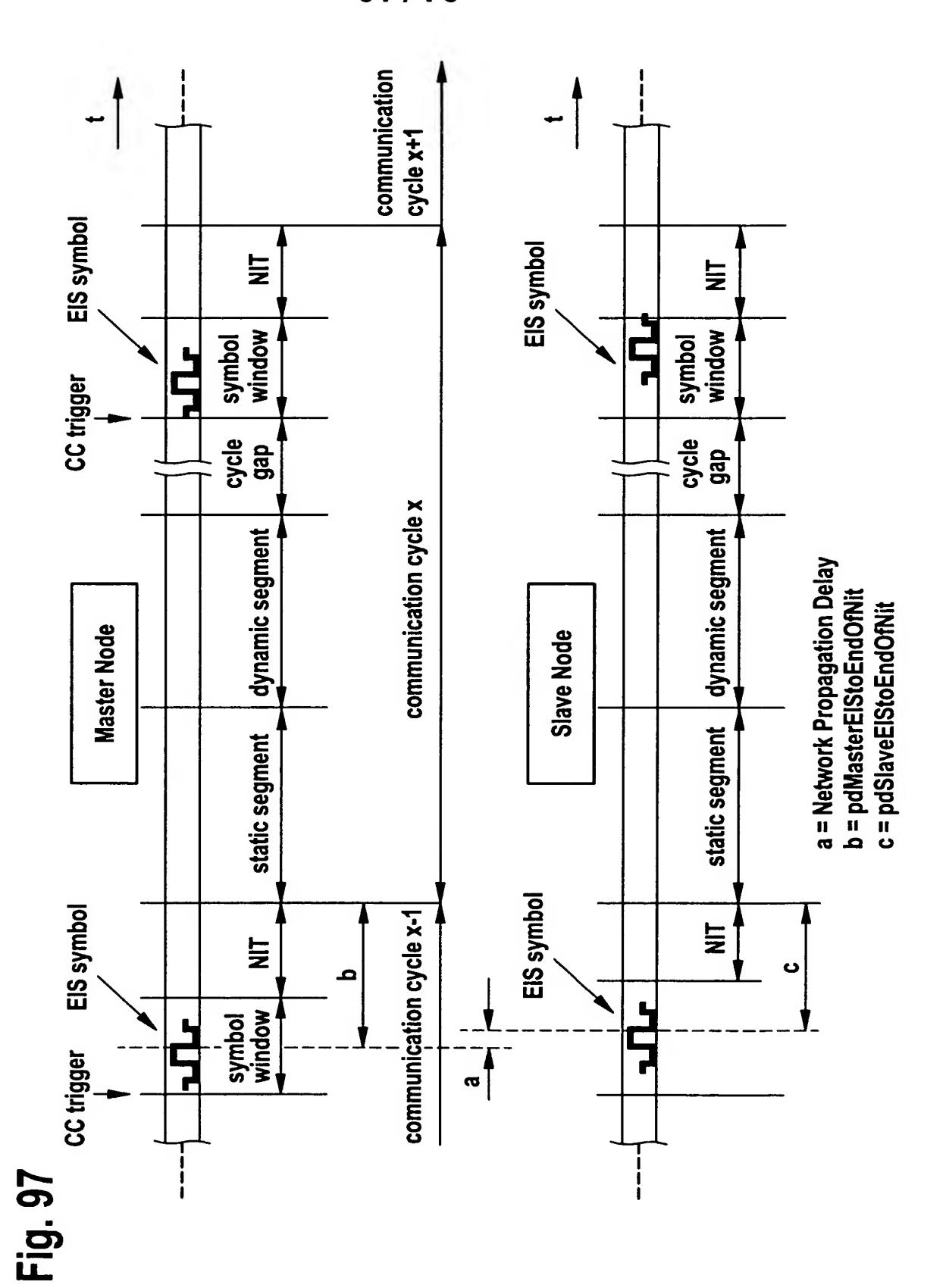


Fig. 95







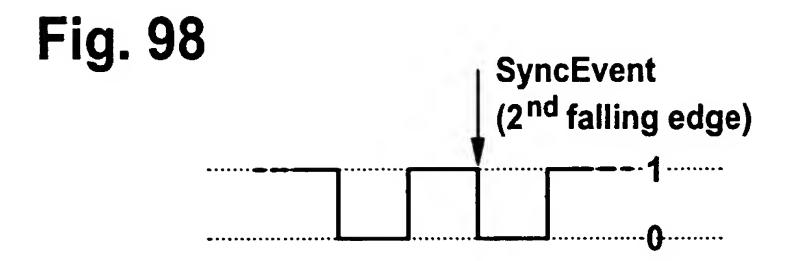
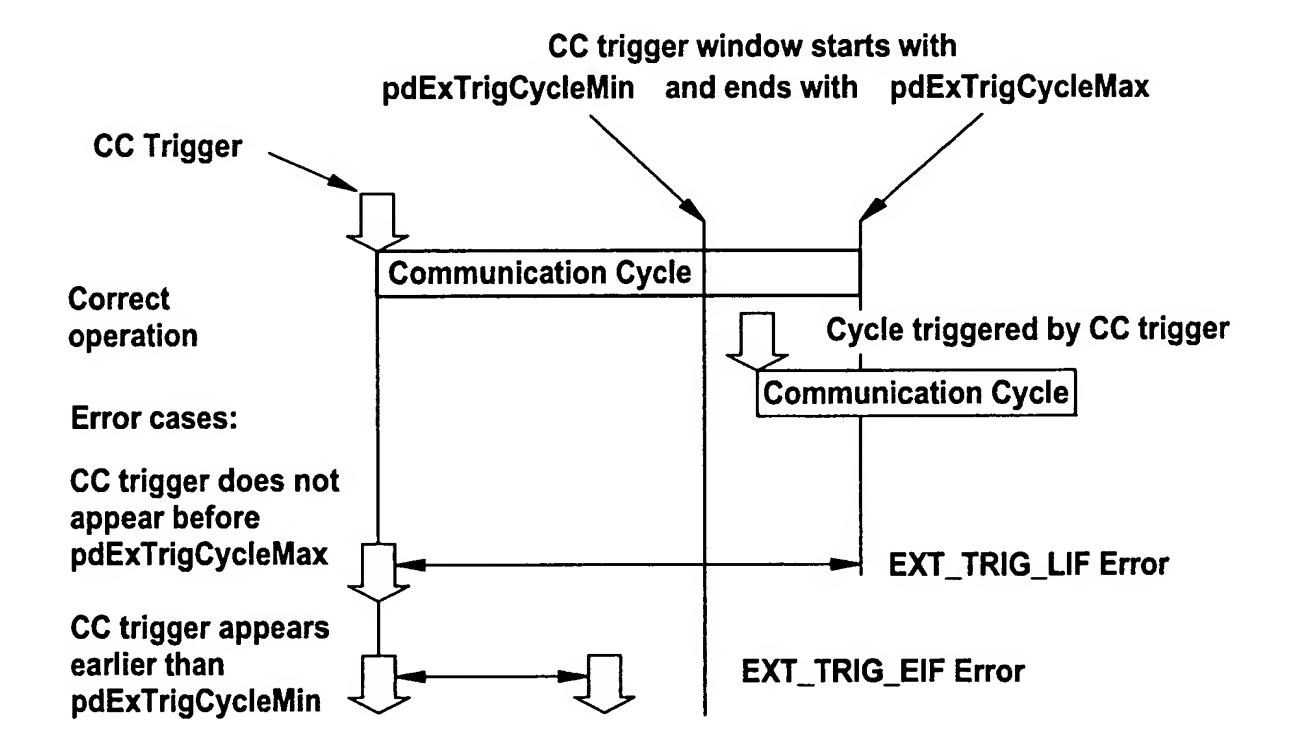


Fig. 99



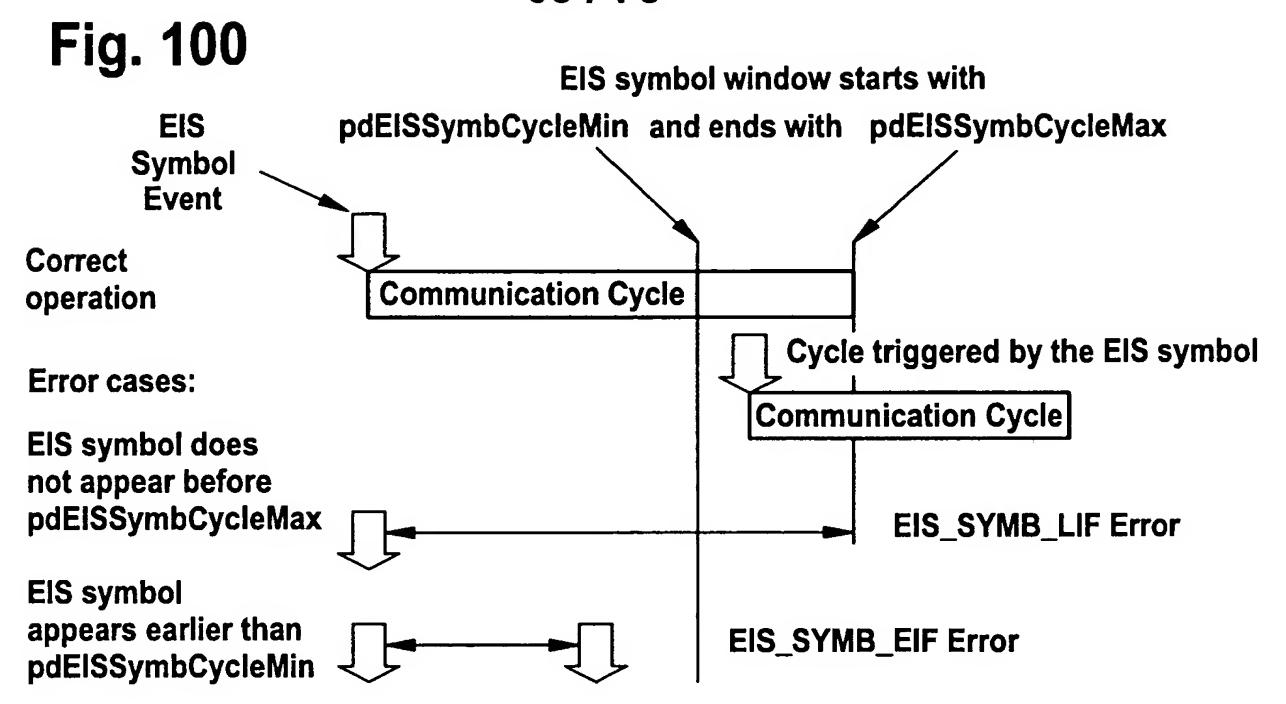


Fig. 101

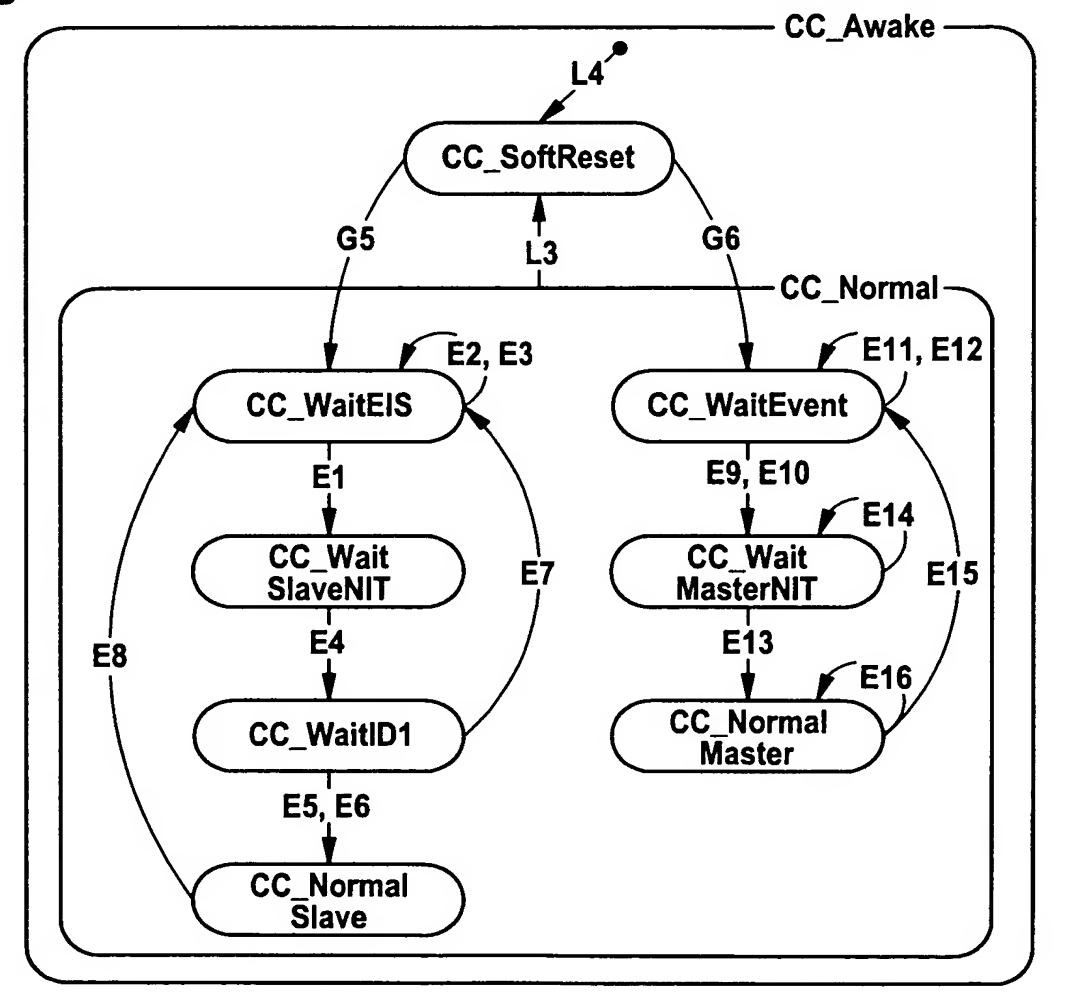
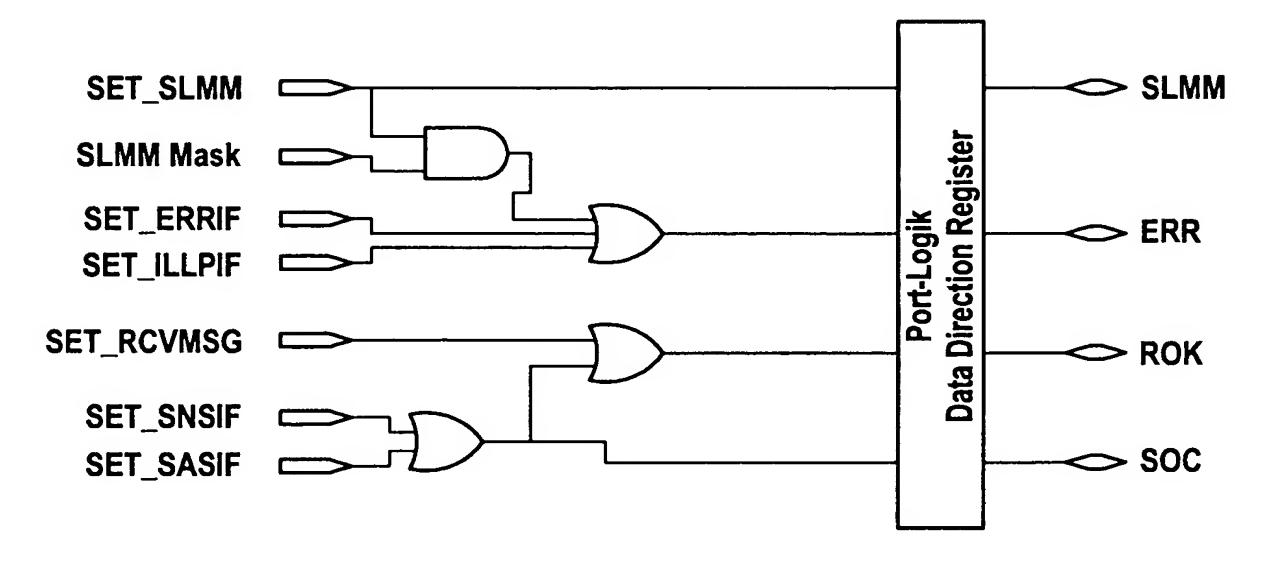


Fig. 102



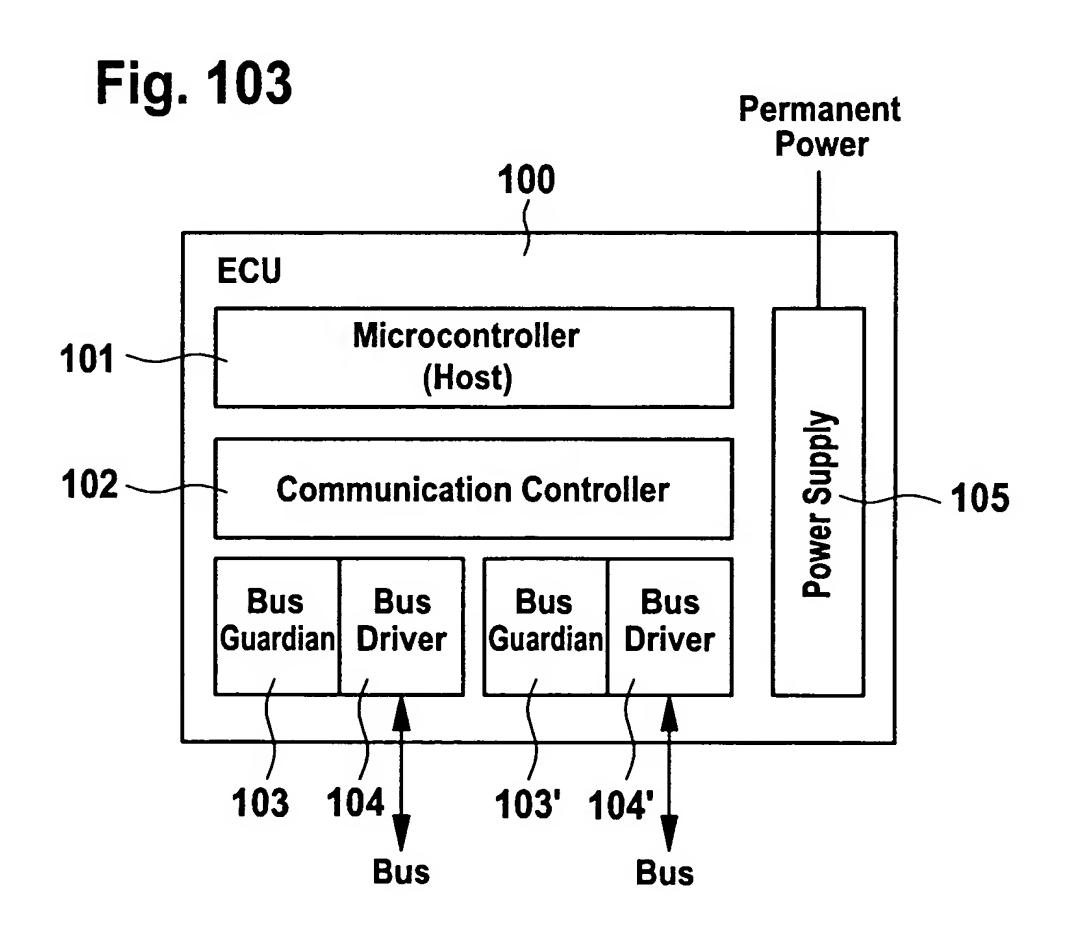


Fig. 104

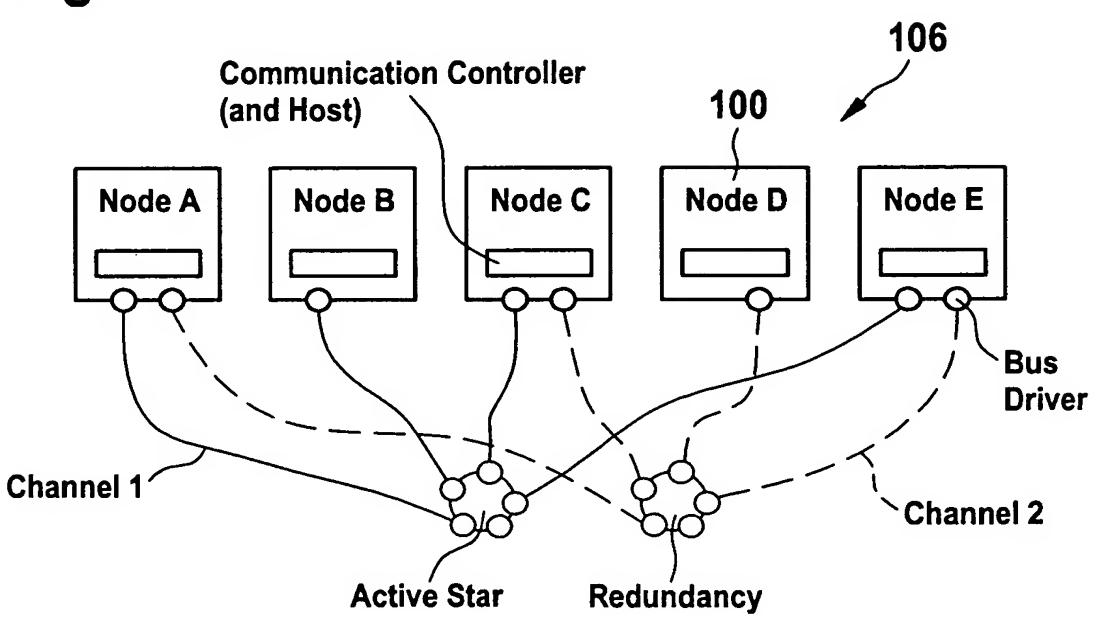


Fig. 105

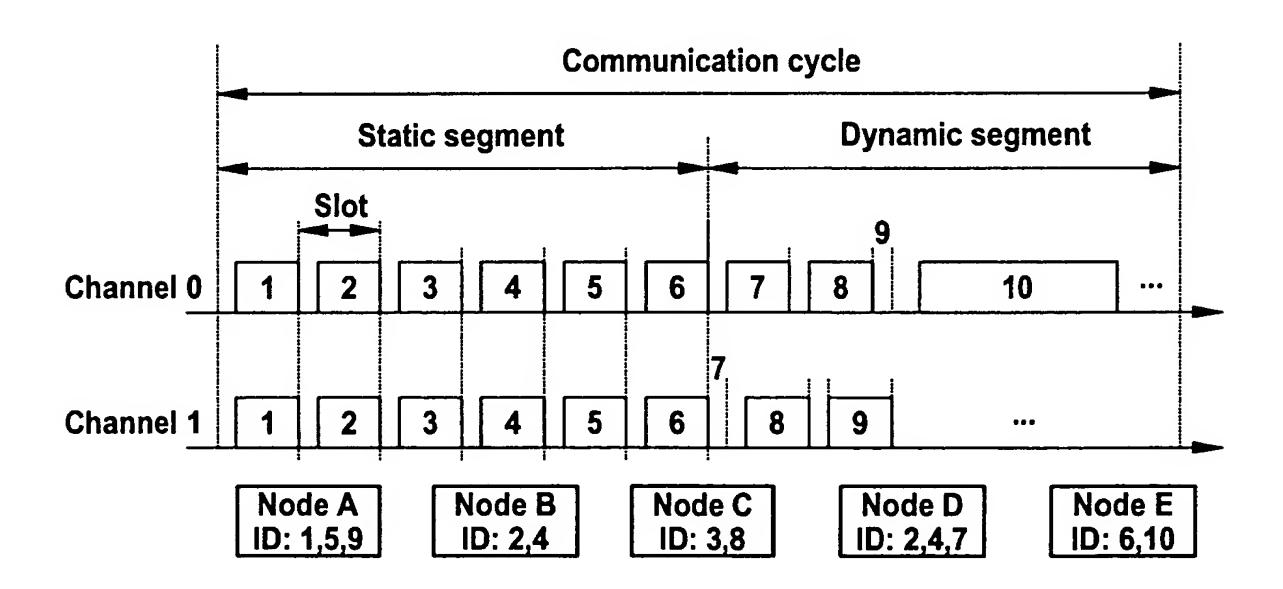


Fig. 106

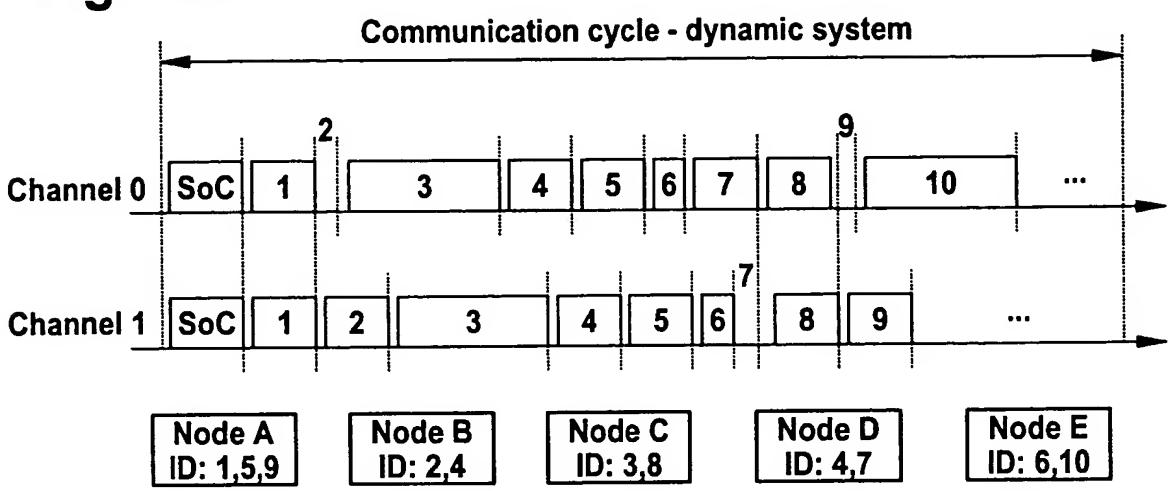
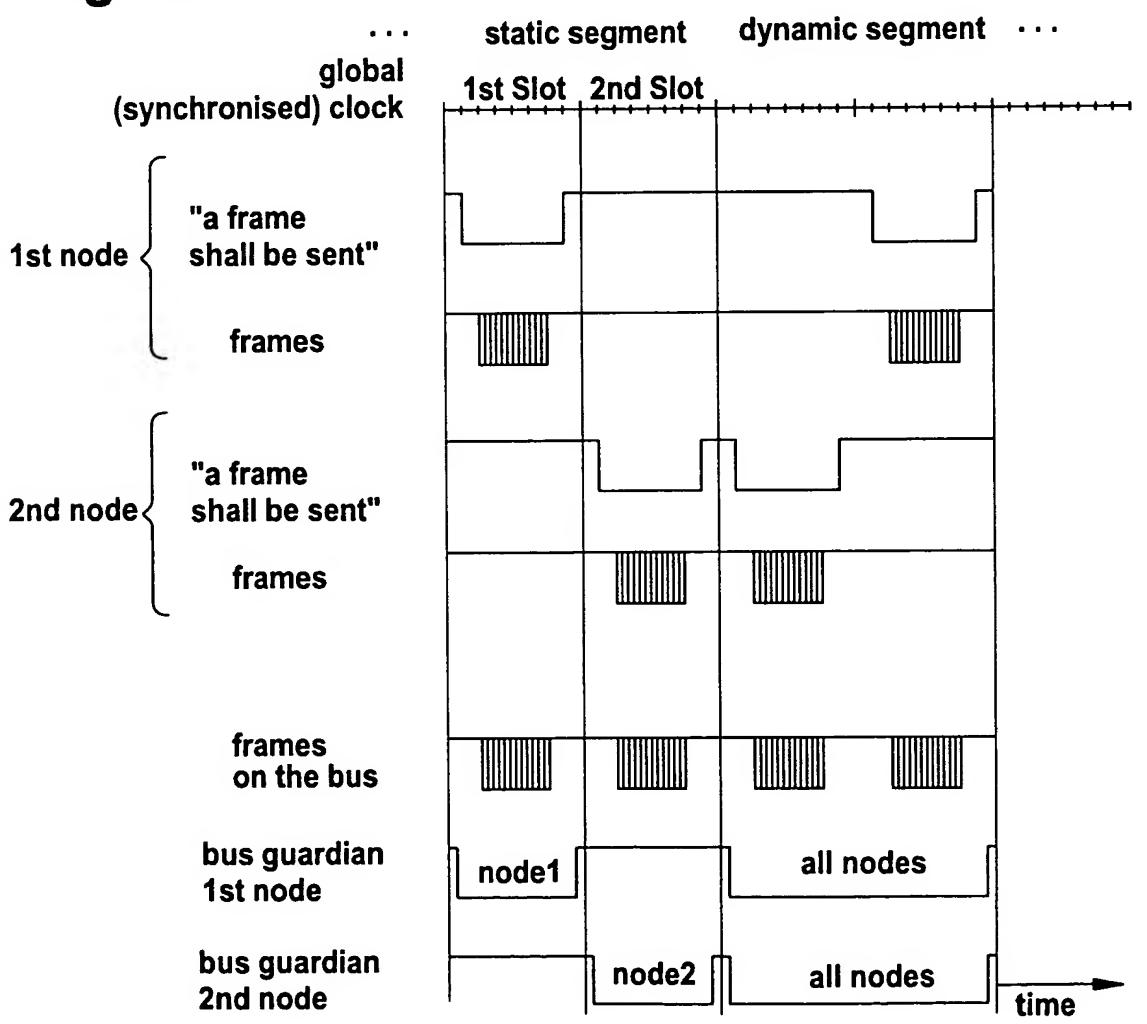
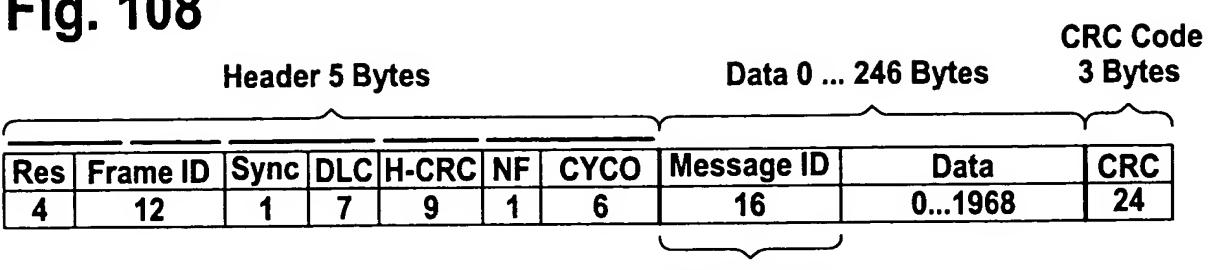


Fig. 107







Configurable

Fig. 109

Header 2 Bytes			Data 0 12 Byte		CRC Code (15 Bit) + Frame Completion Bit	
					ו	
ID	RES	LEN	DATA	CRC FCB		
8	4	4	0 96	15 1	_	

Fig. 110

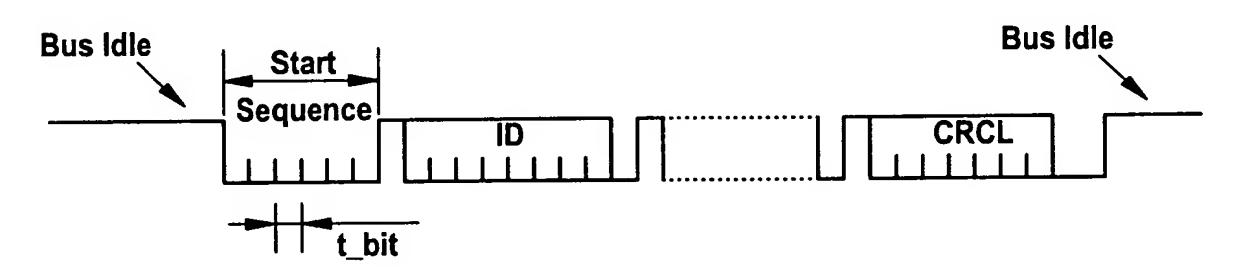


Fig. 111

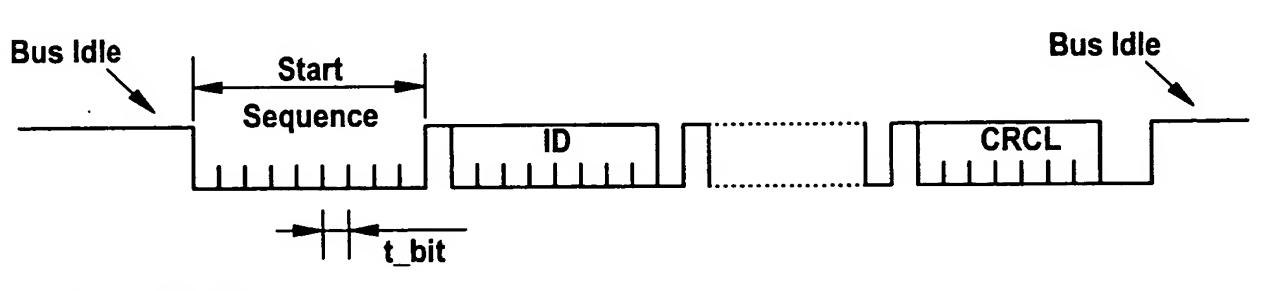


Fig. 112

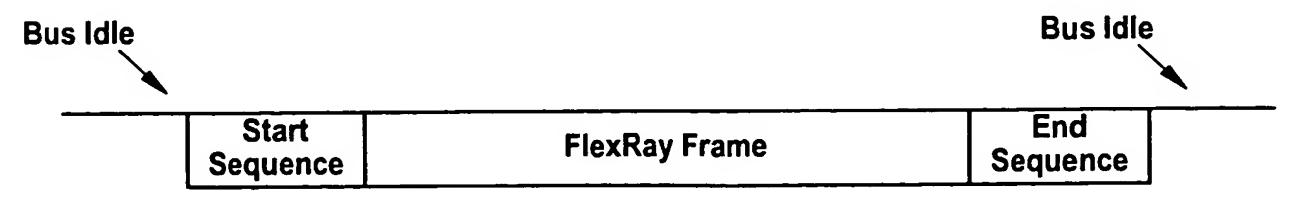


Fig. 113

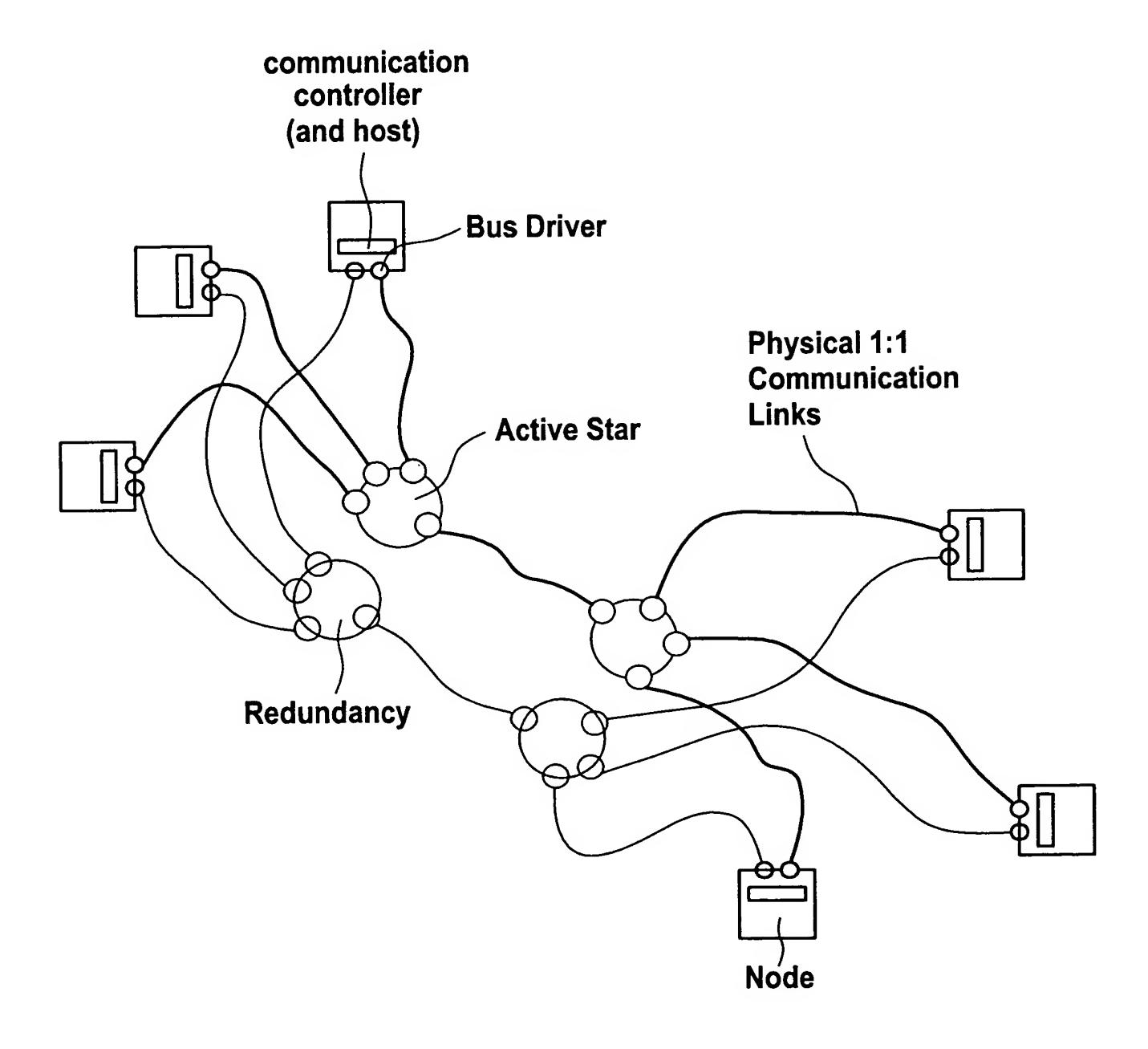
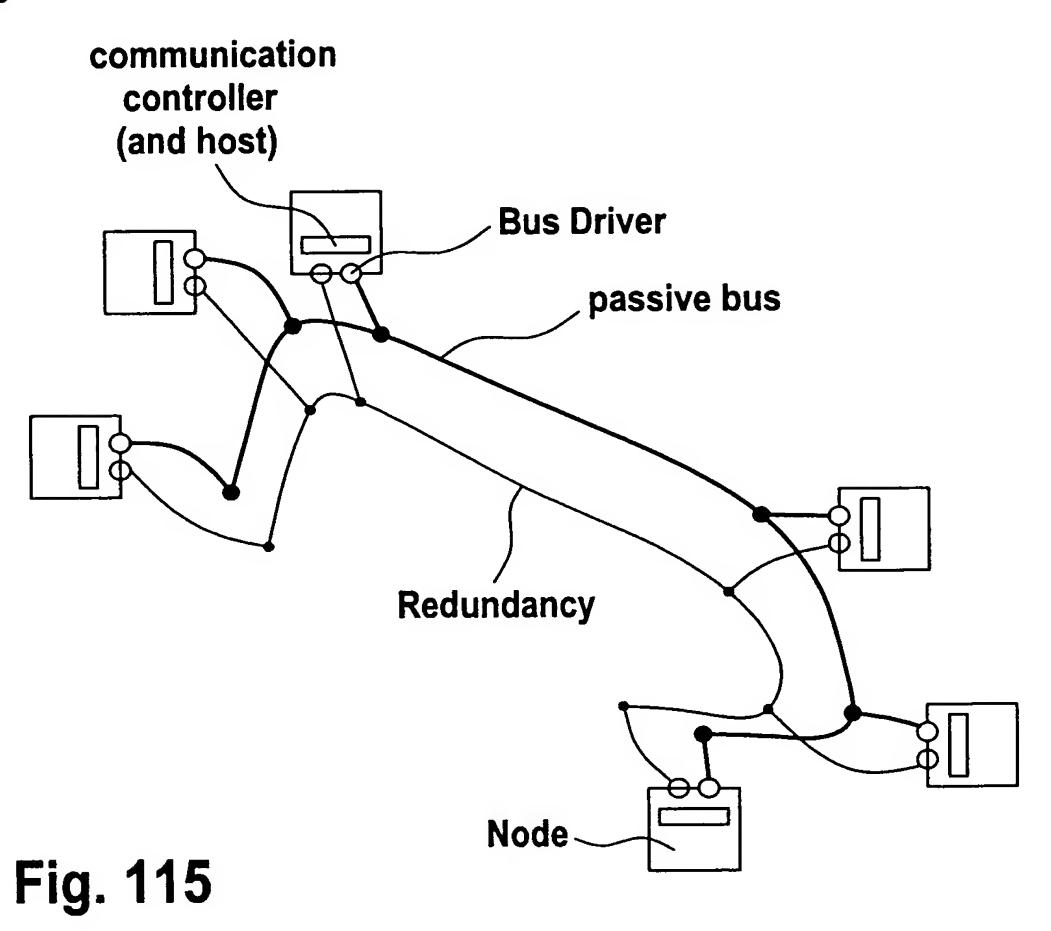
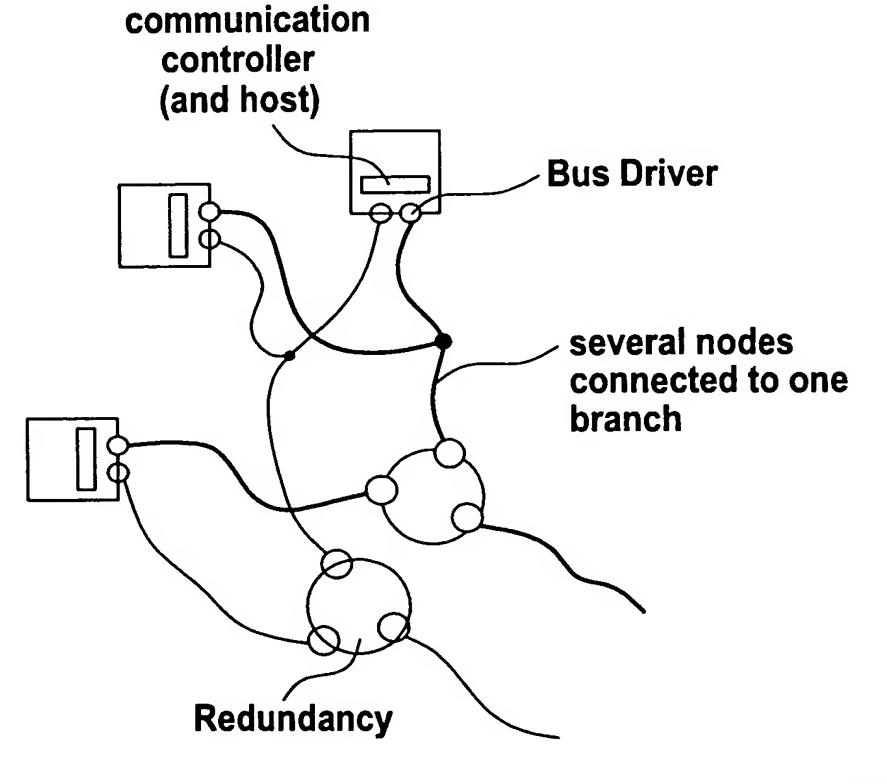
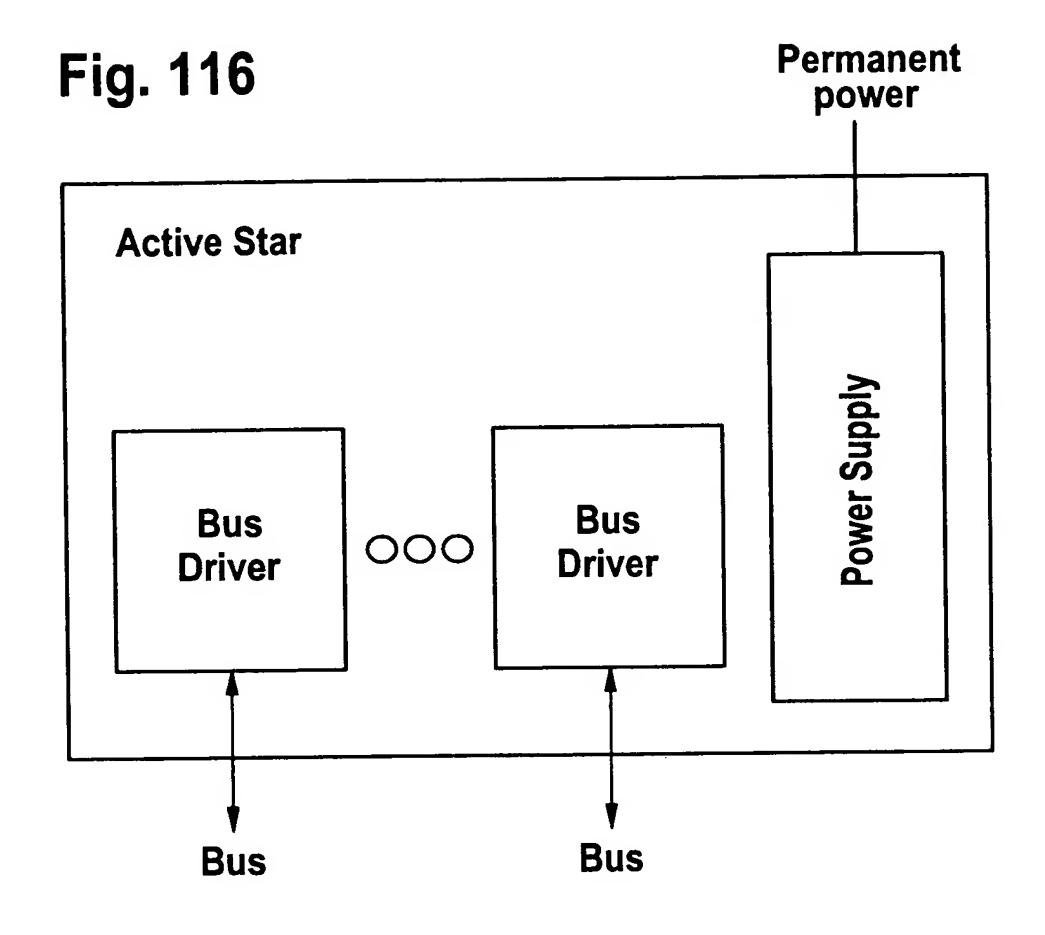
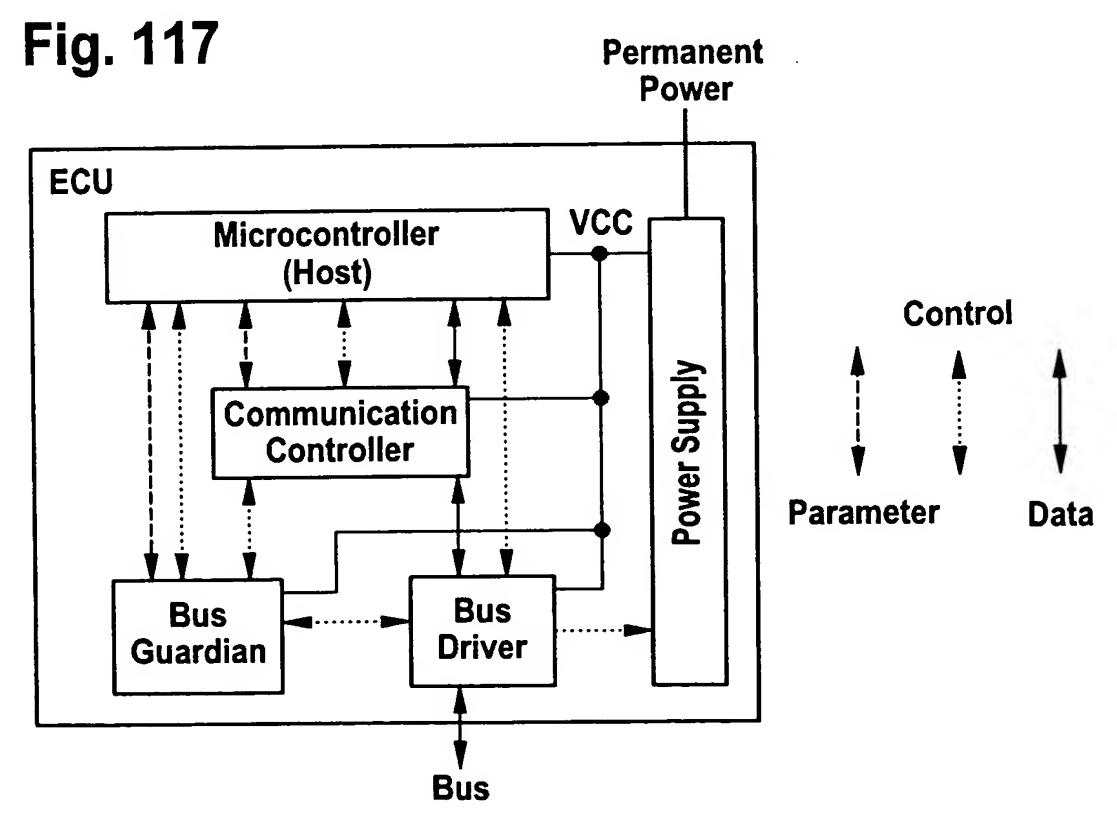


Fig. 114









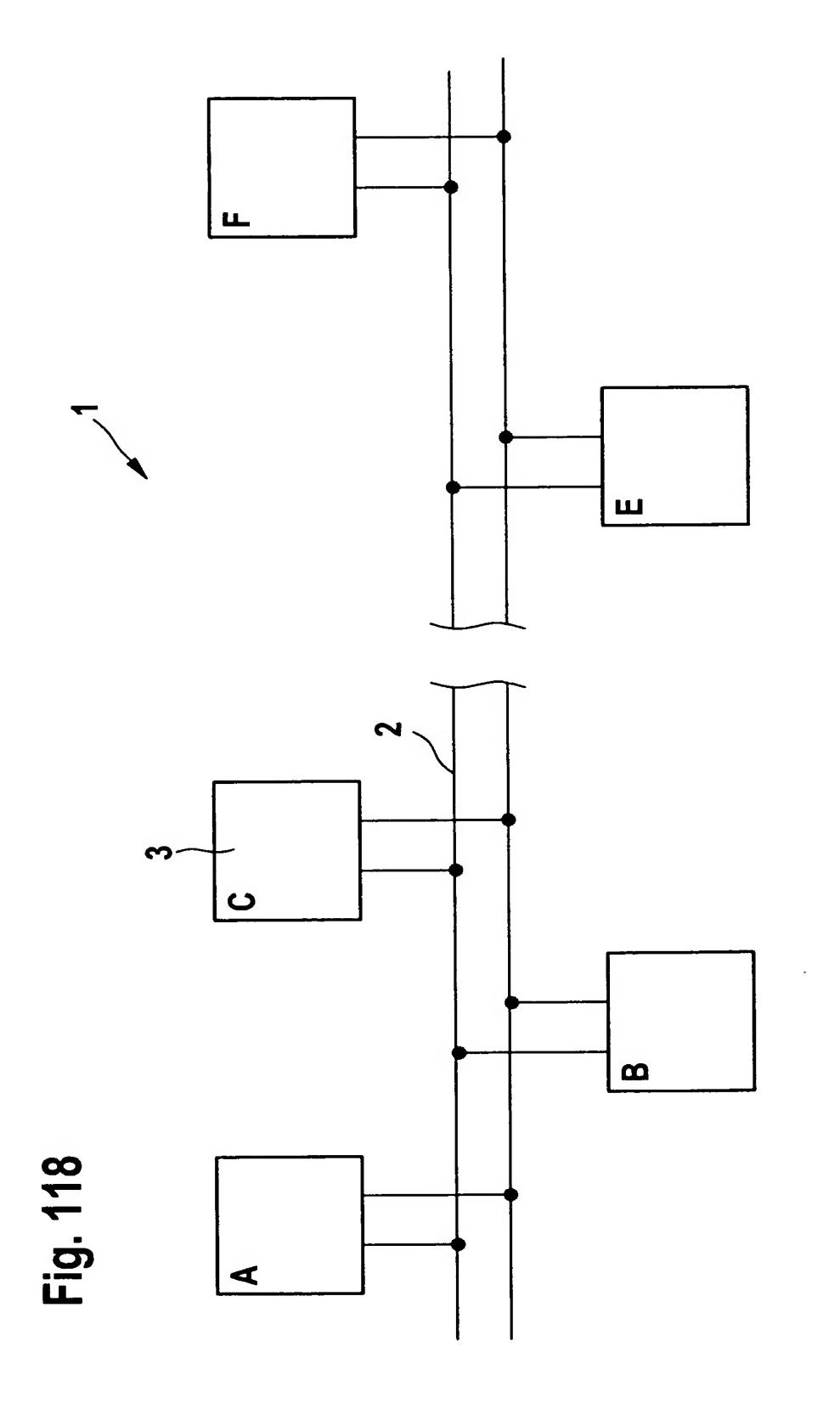


Fig. 119

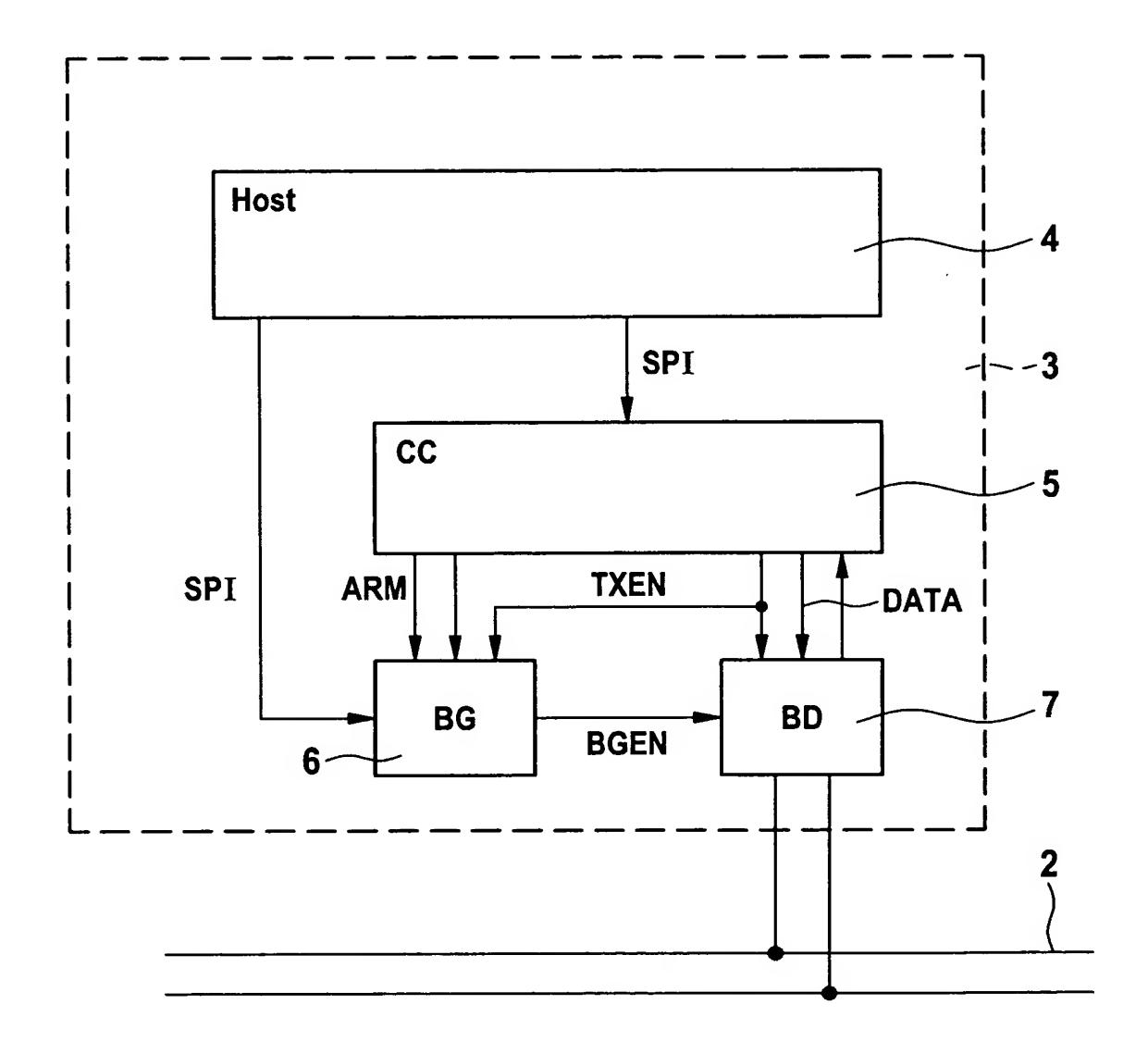


Fig. 120

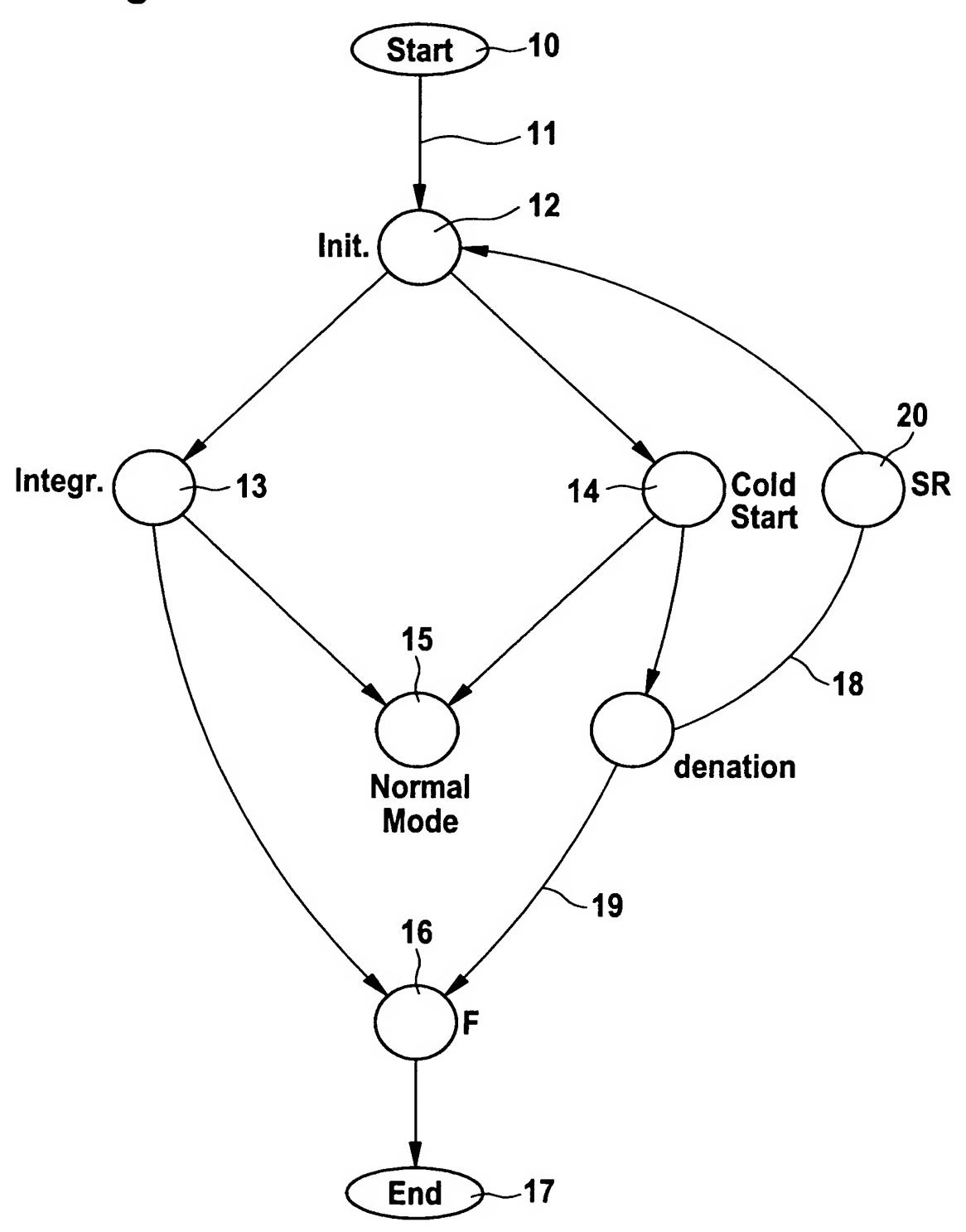


Fig. 121

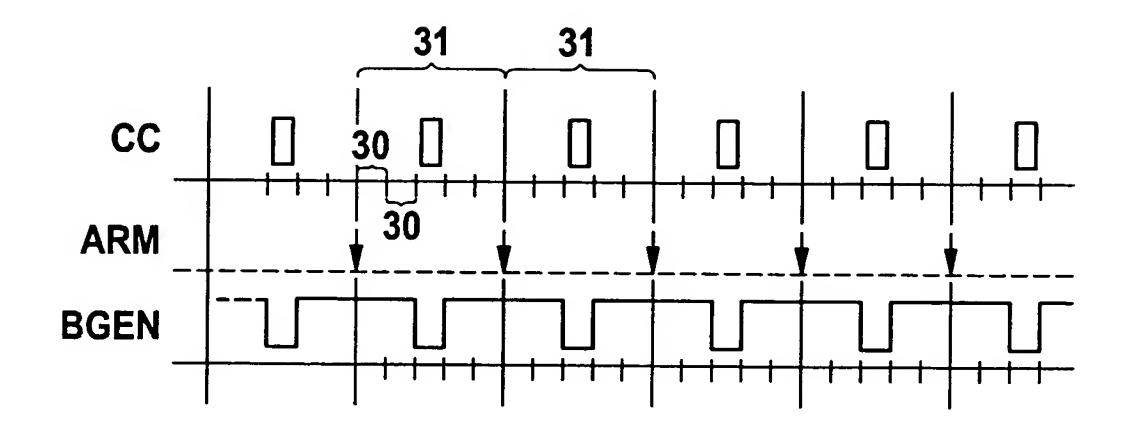


Fig. 122

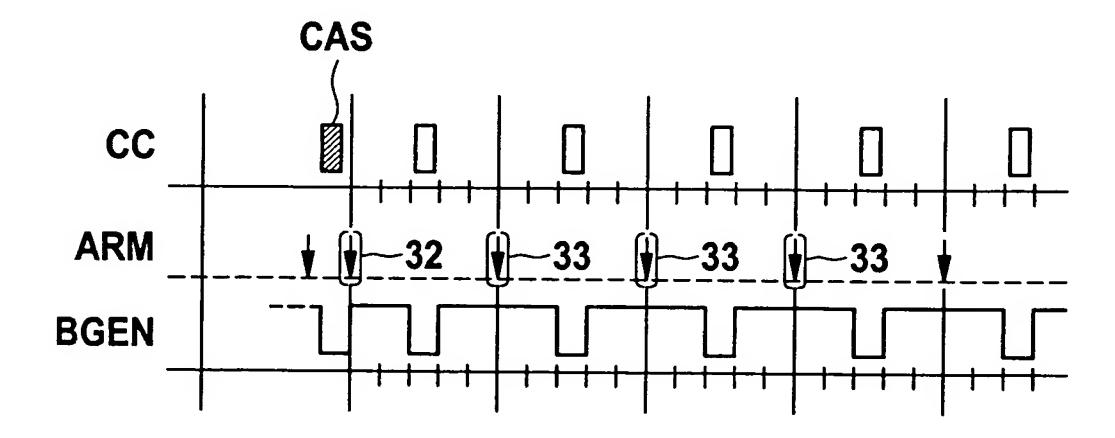


Fig. 123

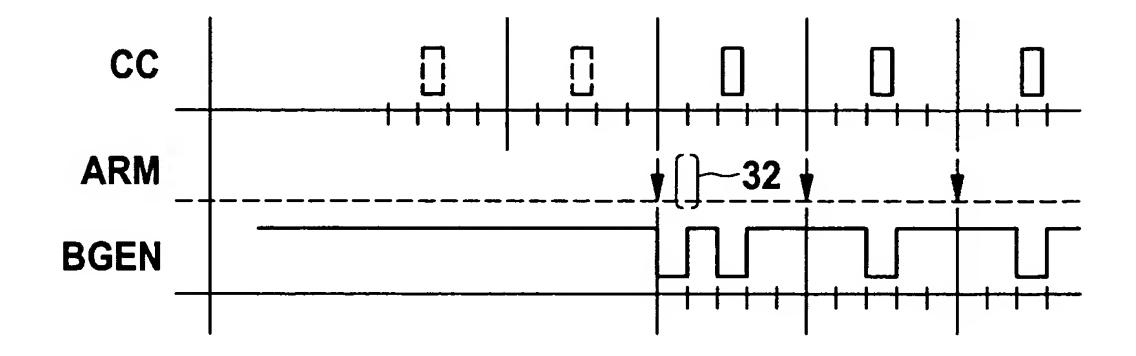
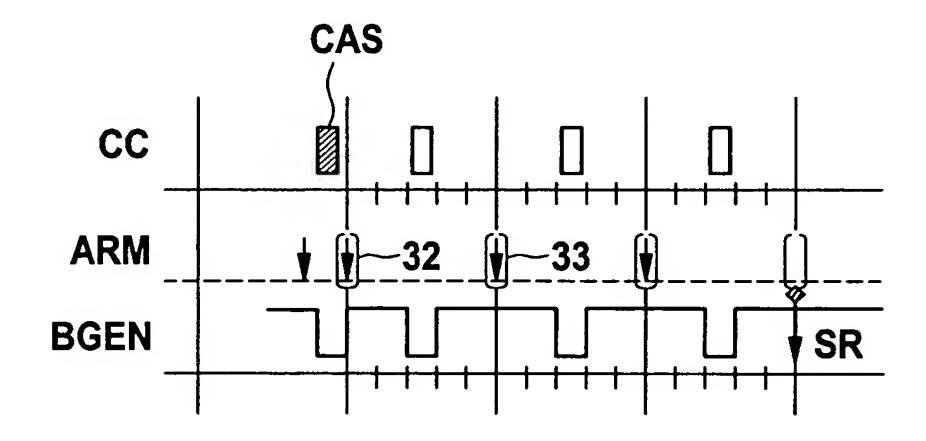


Fig. 124



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Fig. 125

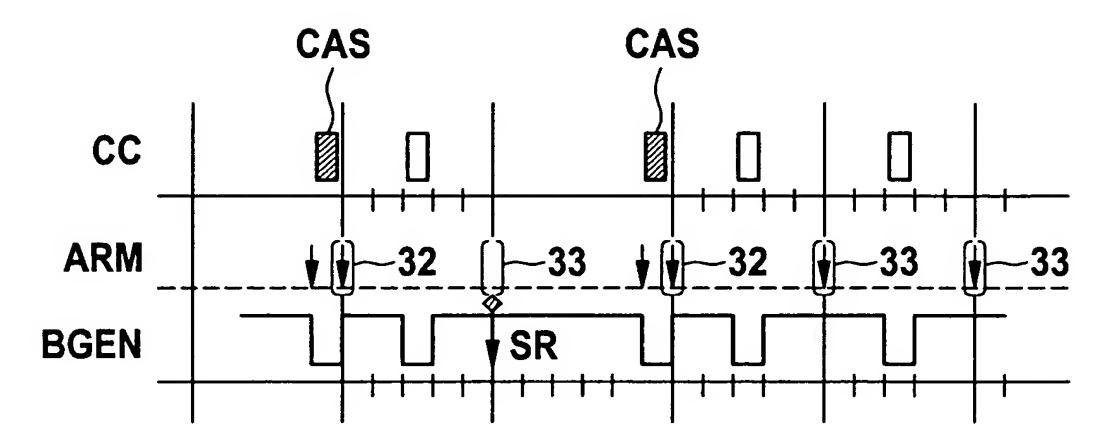


Fig. 126

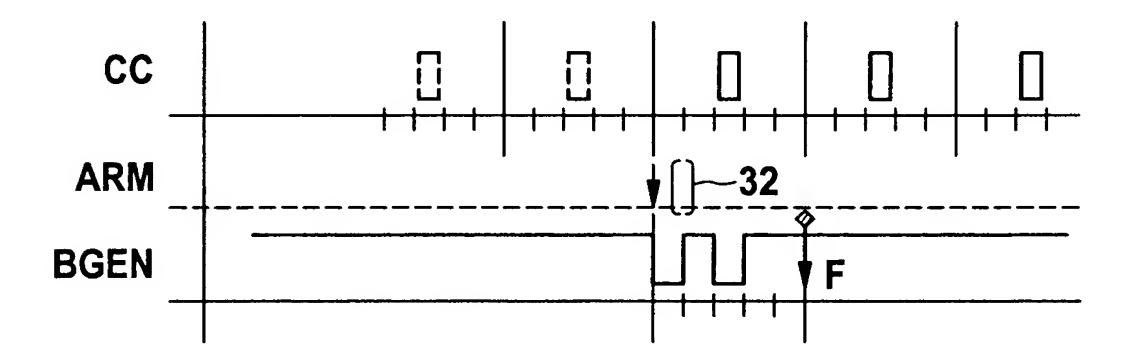


Fig. 127

